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RESOURCE GUIDE 2006

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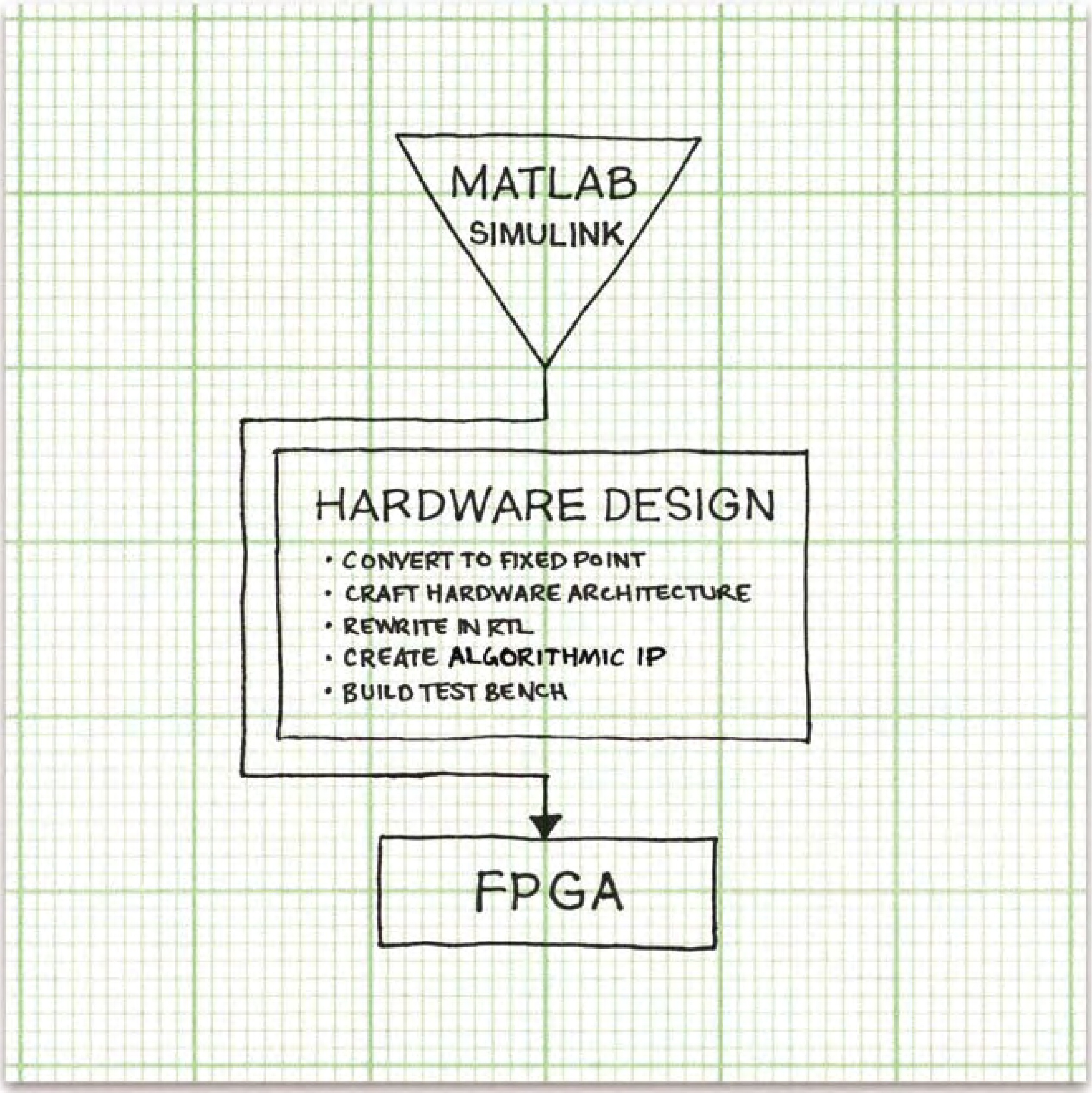

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VOLUME 3
NUMBER 1
2006

COLUMNS

7 Editor's Insight
Two trends I *didn't see*
By Chris A. Ciufo

8 Forward Thinking
High-end DSP markets compute to higher revenue
By Will Strauss

10 Planet DSP
Serial RapidIO (sRIO) architectures in embedded systems
By Robert Oshana

DEPARTMENTS

12, 35 Editor's Choice Products
By Chris A. Ciufo

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FEATURES

15 The future of high-performance COTS signal processing
Hybrid FPGA/DSP architecture: the optimal solution
By Jeffry Milrod, BittWare, Inc.

19 Using FPGAs to combine multiple digital avionic protocol converters in a single board
By Calmon Cozer, BMC Communications Corp.

23 COTS digital radio receiver system is *good to go*
By Daniel McLane, Amit Mane, and Billy Kao, Innovative Integration

27 Interview with Toney Prather
Mid-Tex Cellular deploys real world SDR
By Chris A. Ciufo

29 The benefits of FPGA coprocessing
By Tom Hill, Xilinx

33 The processing challenges in making network-centric warfare a reality
By Neil Harold, Nallatech, Inc.

SPECIAL FEATURES: RoHS

37 *Facing component obsolescence*
Phoenix or a Sitting Duck – what will be your response to RoHS?
By Lawrence Ricci, Applied Data Systems

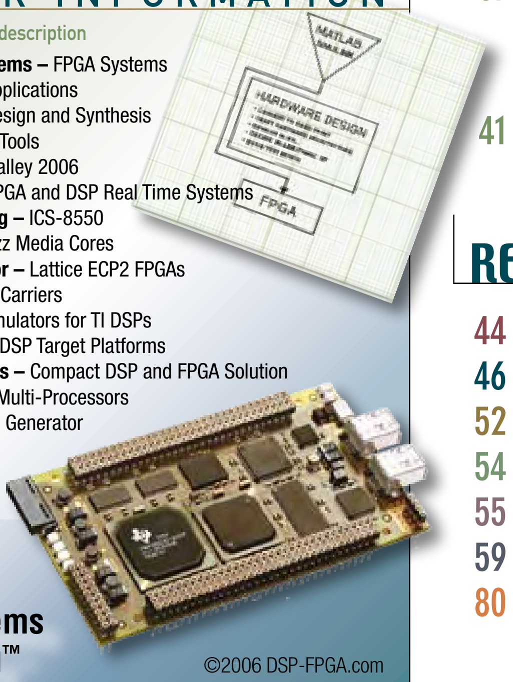
41 RoHS: Yes, it affects *you*
By David Compston, Radstone Embedded Computing

RESOURCE GUIDE

44 Software Defined Radio
46 Software
52 DSP Based Carrier Boards
54 DSP Chips and Cores
55 DSP Resource Boards
59 FPGA
80 Hardware

ADVERTISER INFORMATION

Page/RSC#	Advertiser/Product description
14	**Annapolis Micro Systems –** FPGA Systems
28	**BittWare –** Wireless Applications
32	**Celoxica –** C-based Design and Synthesis
22	**Gedae –** Development Tools
36	**GSPX –** GSPx Silicon Valley 2006
3	**Hunt Engineering –** FPGA and DSP Real Time Systems
9	**ICS Sensor Processing –** ICS-8550
87	**Improv Systems –** Jazz Media Cores
18	**Lattice Semiconductor –** Lattice ECP2 FPGAs
88	**Micro Memory –** VME Carriers
40	**Spectrum Digital –** Emulators for TI DSPs
6	**Spectrum Digital –** TI DSP Target Platforms
5	**Traquair Data Systems –** Compact DSP and FPGA Solution
26	**VMETRO –** Real-Time Multi-Processors
2	**XILINX –** Xilinx System Generator



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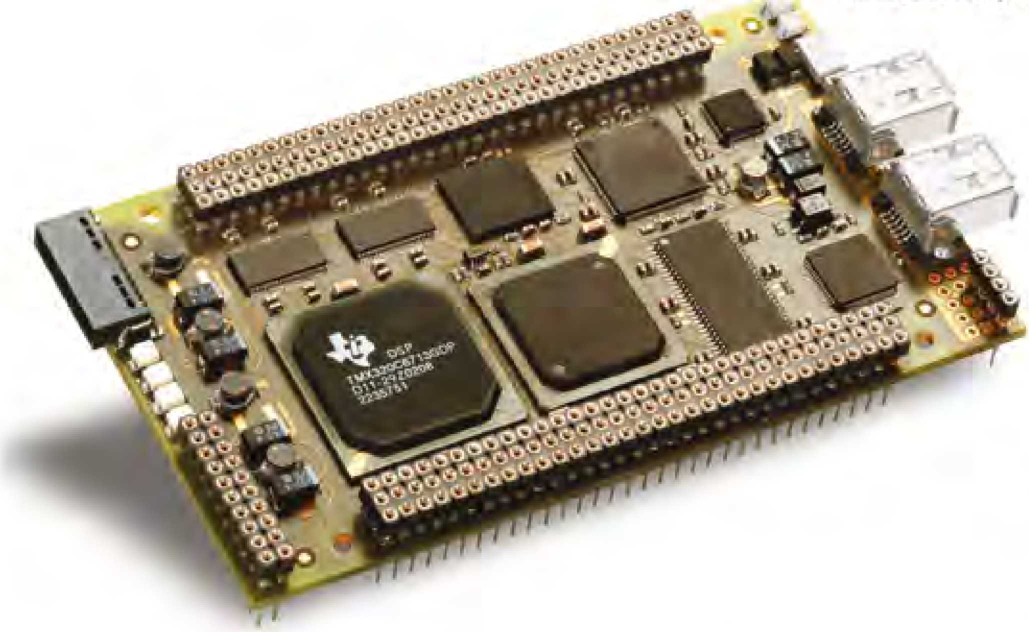

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Two trends I didn't see

Editor's note: This special print issue of **www.DSP-FPGA.com** *comes out only once a year, so we have to cover a year's worth of technology in only 700 words. Check out the website and E-letter for monthly trends.*

By Chris A. Ciufo

Every magazine and blog that covers DSP, FPGAs, and related EDA technologies issues a credible tech trends forecast. Guys like John Blyler at *Chip Design,* Rich Nass at *Embedded Systems Programming,* Kevin Morris at *FPGA Journal*, and even our very own contributing editor Will Strauss of Forward Concepts are all smarter than me. So why risk my reputation by offering the same old predictions you've read elsewhere? Instead, let me reveal two trends I *wanted* to see over the last 12 months but didn't. Each of these could have huge ramifications on the entire industry, if I could only will them into existence. Maybe next year.

FPGAs in cell phones

I know I'll get a nasty-gram from a reader telling me about some FPGA that's already installed in a cell phone design, but I'm referring to a Virtex II Pro-like device slimmed down in price and power. This would enable replacing the ASSP every handset manufacturer relies on for the DSP front end. Even though TI's OMAP and IBM's Power architecture are perfect platforms from which to start a custom design, nirvana will be cheap and reconfigurable FPGAs that would enable true over-the-air programming not just of the firmware and SIM functions like today, but of the *entire handset's radio and user interface*.

Think about this for a minute. In the U.S., handset sales are primarily driven by the carriers. Although you can conceivably buy a network-compatible handset for, say, Verizon and then have it begrudgingly activated by the carrier – friends have told me this is such a hassle it's not worth it. And companies like Sprint and Cingular don't make much money off the handset – they want your recurring monthly revenue and the add-ons like ringtones and picture messages. Getting locked into a 2-year contract irritates consumers (but protects the carrier's subsidies on equipment), and come on – the next handset you buy is rarely that much better than the previous one. So now brown (excuse me, *chocolate*) is the trendy color? But the guts are similar.

They aren't getting much smaller anymore nor is the battery life increasing exponentially. Instead, the next handset usually offers newer features – plus the usual trendy case color. Wouldn't it be better to keep a handset longer but upgrade the feature set? Software defined radios (SDR) would keep the RF portion "fresh", while an FPGA-based subsystem could allow a complete handset reconfiguration. With so much IP available for FPGAs – from better audio codecs than MP3 such as Ogg, to H.264 video – using an FPGA in a cell phone's a no-brainer.

Alas, for now all that performance, density, and I/O comes at the expense of, well, power and expense. Xilinx swears they're not eyeing this market, but some of their Spartan-3 announcements and feature enhancements make me wonder. And Lattice is feverishly working their way *up*-market with their ECP2M family and recent LatticeMico32 architecture. Lattice might move up faster than Xilinx can move down. Optimizing SWAP (size, weight and power) in cheaper FPGAs would reverberate across the entire embedded market, not just cell phones.

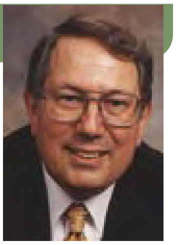
Still too darned complex

DSP relies on complex math – and I do mean *I* and *Q*. But unlike running code on microprocessors, where the software engineer doesn't have to worry about race conditions, silicon fan out, or gated clocks, why the heck do DSP designers need to worry about hardware-level issues? I mean, FFTs , FIRs, and twiddle factors are complex enough. But designing with DSPs – despite the best efforts of companies like The MathWorks (Simulink and MATLAB) - tools only solve a piece of the bigger system problem. And the new trend towards *Electronic System Level (ESL)* design at least steps back a bit to look at the bigger picture, but it's usually narrowly focused on sub-system details such as a single device.

To me, this is all still too micro. John Blyler, editor of *Chip Design* did a great job of summing up ESL's complexities in his June/July 2006 issue. But that's just it: it's still too complex. I had hoped that 2006 would start to move the industry away from "coding at the metal" while being forced to deal with the nuances of transistors and floorplanning. Think about it – when you use Windows programs are you expected to know how to *write them?* Need you modify the registry just to get Excel to calculate a large spreadsheet?

We need much higher level system-level tools that mask the details of the silicon as well as the details of DSP's mathematical constructs. For me, I'd be happy with a bunch of Eclipse-like open source tools that designers "drag and drop" together to help create, simulate, and validate systems. Alas, I don't see much movement in that direction yet since the industry's mired down in the details of ESL, DSO, and other anthills. Fixing this problem might take some of the mystery out of designing embedded signal processing systems – by hiding the details only experts need to worry about.

High-end DSP markets compute to higher revenue



By Will Strauss

Digital Signal Processing (DSP) is a technology that has become pervasive and touches our lives daily. It's used in our multimedia world of MP3s, DVD players, and digital TVs, to our connected world of cable, DSL, and Wi-Fi modems. These technologies give us access to the Internet, and in cell phones that provide unprecedented mobility, allowing us to reach out and touch someone anywhere, anytime. From a DSP standpoint, many of these applications don't require very much processor horsepower. MP3 decoding, for example, seldom requires a dedicated DSP chip. Just about any low-end RISC chip with a hardware multiplier can do the job.

But, there are DSP applications that require an order of magnitude greater processor capability. Instead of the 50 MMACS (million multiply-accumulates per second) or so required for MP3 decode, there are applications that require several billion MACS or more. The highest-performing DSP chips now available are rated at over 8 GMACS for a single core. Although that's fast enough to address a significant number of high-performance applications – there are even higher-end markets that require multiples of those fast DSPs combined with FPGAs, even multiple instances of both. FPGAs capable of over 100 (18-bit) GMACS are available, so their high-end DSP market presence is assured.

And what may be characterized as a hybrid approach combining FPGA-centric interconnection techniques with collections of processor cores (instead of logic gates), new massively-parallel arrays of elemental processors are now coming to market to serve DSP applications. With as much as 60 GMACS capability and real-time logic reconfigurability, some of these processor arrays are targeting software-defined radio (SDR) applications while others target professional multi-channel, multi-standard video codecs.

Obvious examples of high-end DSP applications include volumetric medical imaging, like MRIs and CT scanners. Early versions of these products were able to scan and later display 3D images over a matter of hours. Newer ones do it in a matter of minutes, and both doctors and patients want them in seconds. All of these scanners require an array of processors to perform the faster processing. High-end DSP chips have also enabled ultrasound scanning in doctor's offices, eliminating the inconvenience of hospital trips for many patients.

Other forms of high-performance scanning include military radar and sonar. These applications can involve dozens of high-performance DSP chips or MPUs with DSP-centric vector coprocessors. And that's in addition to the beamforming DSPs required for electronically-steerable antennas and transducers.

In our latest survey of DSP professionals, we asked participants, "What is the typical DSP performance requirement (in 16-bit MMACS) for your organization's primary DSP-centric product?" The results indicated that there is still a very healthy market for low-end DSPs rated at under 100 MMACS (see Table 1 and Figure 1), but we noted a comparable number of respondents indicated that more than 10,000 MMACS (10 GMACS) were required for their high-end application. Cross-tabulation with answers from other questions indicated that most of those high-end responses involved multiple chips, with as many as 6 chips cited among our survey participants, some with multiple DSPs, others with stand-alone FPGAs and some with combinations of the two. However, several responses indicated single-chip implementations of massively-parallel processors.

HIGH-END DSP MARKETS

- Medical Imaging
- HDTV Studio Encoding
- Video Transcoding
- Video Encryption
- Cellular Base Stations
- Media Gateways
- Radar & Sonar
- Explosives Detection
- Electronics Intelligence
- Satellite Video Transmitters
- Wafer/Reticule Inspection

Table 1

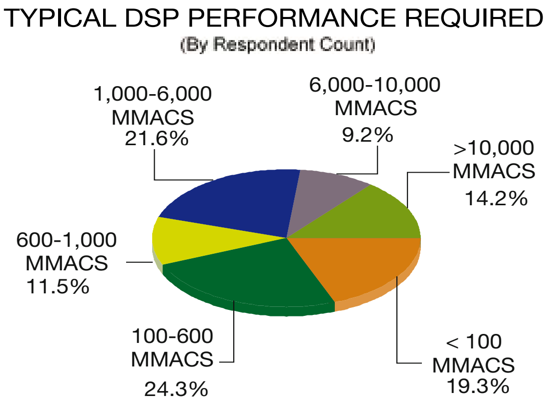


Figure 1

Since DSP algorithms are among the most parallelizable (compared with data processing), arrays of parallel processors can make a lot of sense for high-end applications. The key to a successful product of this type is simply the software development and support tools. Graphic algorithm development tools like MatLab and LabView as well as C-language algorithm libraries are common denominators in the DSP world. The ability to map these into new parallel processor array tools can determine the ultimate market success of such products.

In short, if you can't easily program it, the market won't accept it. The poster child for product non-acceptance would be TI's TMS320C80 (a.k.a. MVP) of the last decade. With multiple RISC and DSP engines, it was the most powerful DSP chip on the planet ... for the three people who could program it. TI learned the lesson well and its new DaVinci™ multi-core architecture for multimedia applications has become a resounding success.

One final point. The average price of a DSP chip today is $5.70, an average heavily weighted by the 900 million or so DSP basebands shipping in cellphones this year. High-end DSPs, on the other hand, sell for hundreds of dollars, while high-end FPGAs can cost several thousand dollars. Consequently, the high-end DSP market is best understood in total revenue, not units. Of this year's predicted $25 billion DSP-centric chip market, Forward Concepts sees the high-end DSP market as a $2-billion opportunity for chip companies that can fulfill industry's needs.

For more information, visit www.fwdconcepts.com/markets.htm.

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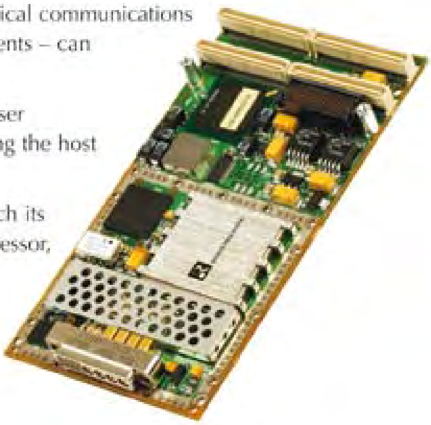

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Serial RapidIO (sRIO) architectures in embedded systems

By Robert Oshana

Modern embedded applications are dramatically driving performance requirements, which need sophisticated, direct peer to peer communication, high reliability, quality of service, distributed processing topologies and interoperability. High performance digital signal processors (DSPs) with fast and flexible IOs are needed to meet these real-time processing challenges of today's applications. Embedded devices are now integrating industry-standard Serial RapidIO (sRIO) bus technology on-chip to provide high-performance, packet-switched, interconnect technology that addresses the industry's need for reliability, higher bandwidth and faster bus speed. This open standard, high bandwidth and system level interconnect decreases overall system cost by reducing the need for additional devices used for switching and processor aggregation.

Understanding necessary requirements for multiprocessing

Embedded systems contain multiple processing elements spread across a single system-on-chip (SoC) device. These processing elements perform different functions of the overall application, including signal processing, data processing and control functions. There are also systems with many discrete processing elements on different devices spread across a board. These devices must communicate to share data and status with each other in order to complete the system processing task. With more devices comes more communication lines, and this drives requirements for communication interconnect between processors.

Interconnect requirements fall into two classes: functional and non-functional. Functional requirements include things like peer to peer communication and support for different device topologies. Non-functional requirements deal with low latency demands, scalable bandwidth and emergent requirements, which refer to reliability, flexibility and efficiency (in terms of performance related to both hardware and software) concerns. Flexibility is of particular importance because there are many system design alternatives depending on the application space.

RapidIO for interconnect problems

Today, there are a few common strategies that address the need for internetworking including:

- Bridging: external devices perform protocol and physical translation.
- Flexible interfaces: device capable of being configured to support multiple interconnects and busses.
- Device versions: chip manufacturers release devices tailored to support different interfaces.

Many multi-processor algorithms, such as DSP algorithms, depend on the flow of large data sets among the various compute nodes that share a problem. Often, the performance of the transfers across the system interconnect limits the overall system performance. One solution to this interconnect problem is RapidIO (RIO, www.rapidio.org). RapidIO is an industry-standard high-speed switched-packet interconnect that is becoming more common in embedded systems to support the demands of applications which require this model of interconnect and communication. The main design goals of the RIO are to offer a light-weight protocol, limit software impact on the system CPU and focus on 'inside-the-box' communications. This widely compatible architecture provides reliable high-performance, packet-switched technology at increased bandwidth for chip-to-chip as well as board-to-board communications (Figure 1).

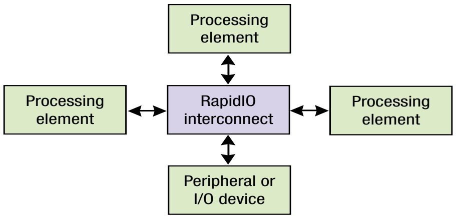

Figure 1

In order to allow scalability and future enhancements while maintaining backward compatibility, RapidIO has a three-layered hardware architecture: physical, transport, and logical. More specifically, this allows the flexibility of adding new transaction types to the logical specification without requiring modification dto the transport or physical layer specifications.

The *physical layer* is the electrical signaling and link level handshaking mechanisms as well as CRC based error detection. RapidIO is a parallel interface that is either 8 bits or 16 bits wide and runs at 250 MHz to 1 GHz with data clocked on both edges. The *transport layer* dictates how packets are routed in the switched environment. RIO uses a destination based routing to route packets to the correct device based on a device ID embedded in the packet. The *logical layer* is the highest layer which defines packet types and function. RIO can have up to 256 byte packet payloads.

On-chip serial RapidIO

There is a serial version of the RapidIO technology as well. Serial RapidIO, is a point-to-point switched serial interconnect. sRIO is *physically incompatible* with parallel RapidIO technology so the developer must select the exact mix of parallel and serial connections. The signaling rate for sRIO is 1.25, 2.5, or 3.125 Gbps per differential transmit and receive pair (these are also called *lanes*). This provides up to 312.5 MBps in each direction per lane. Each SRIO port is configured as one or four lanes which can provide a maximum data rate of 1.25 Gbps per port.

sRIO makes it easier to support multiprocessing and eliminates the need for aggregation logic with its ability to support variety of topologies. For example, in video infrastructure applications, the physical layer data transmission uses SERDES (analog serializer/deserializers) technology to perform clock recovery from the data stream and incorporates 8B/10B coding. The serial specification supports 1-lane (1x) and 4-lane (4x) port sizes. A 1x sRIO link is fast enough to send two channels of HD 1080i raw video between devices and a 4x link can easily send four channels of HD 1080p raw video between devices with bandwidth to spare.

This serial architecture provides a maximum payload of 256 bytes per packet and does not provide the scalability of other interconnects like PCI Express or parallel RIO. For instance, in computing applications, the PCI bus is frequently used to connect multiple disk channels to a system. As disk throughput increases, so does the need for high system throughput, which can be achieved with higher bus frequencies. This leads to a smaller number of supportable devices per bus segment, but in order to connect the same number of devices, more bus segments are required. PCI-to-PCI bridge devices could be used to solve this problem but only within a tree-shaped hierarchy that increases system latency and cost as more PCI devices are added to the system. Instead, higher system level performance can be achieved by using RapidIO. RIO's point-to-point topology enables the removal of devices with little or no electrical impact to neighboring devices or subsystems.

As an example of the growing use of RIO and sRIO in embedded applications, Texas Instruments' TMS320C6455 DSP device (Figure 2) supports a sRIO bus interface. This interface can boost performance and I/O bandwidth in high-end and multichannel applications such as video and voice transcoding, videoconferencing servers, high-definition (HD) video encoding, and wireless base station transceivers. System performance can be increased up to 12x because sRIO eliminates IO bottlenecks by providing a low latency, high bandwidth (10 Gbps full duplex), and low pin count interconnect. The on board sRIO can also provide communications connectivity to third party tools, FPGAs, sRIO switches, and sRIO equipped embedded processors.

Software and infrastructure

In addition to the raw performance offered by sRIO, software developers can also develop applications without having to do a lot of low level device programming. Several embedded processor vendors provide support for sRIO in the kernel level software layer. For example, TI's RTOS and DSP/BIOS software kernel foundation have a sRIO Message Queue API which allows application developers to development software applications at a higher level of abstraction.

The use of sRIO in infrastructure applications with large "DSP farms" will also lead to a reduction in system cost in terms of device count, board size and/or device cost. For example, embedded systems development now includes the increased use of Direct Memory Access (DMA) as well as other smart peripherals that can move data at extremely high rates. The current multi drop interconnects cannot support the required bandwidths without using more signals/pins and connectors which increased overall system cost. sRIO with its DSP farms overcomes these problems without affecting the cost.

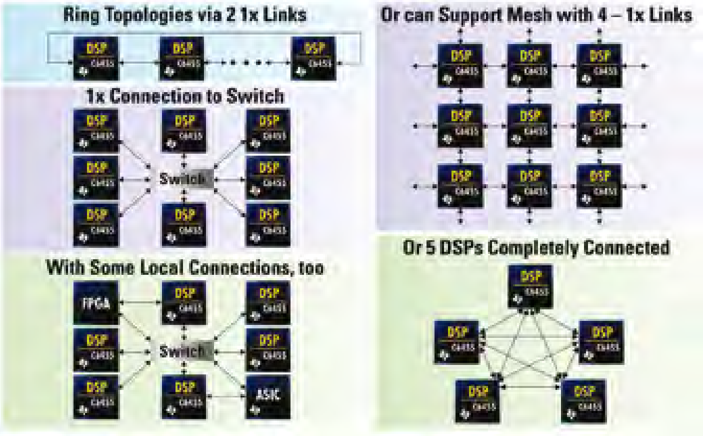
Ring Topologies via 2 1x Links
Or can Support Mesh with 4 – 1x Links
1x Connection to Switch
Switch
With Some Local Connections, too
FPGA
Switch
ASIC
Or 5 DSPs Completely Connected
DSP
C6455

Figure 3

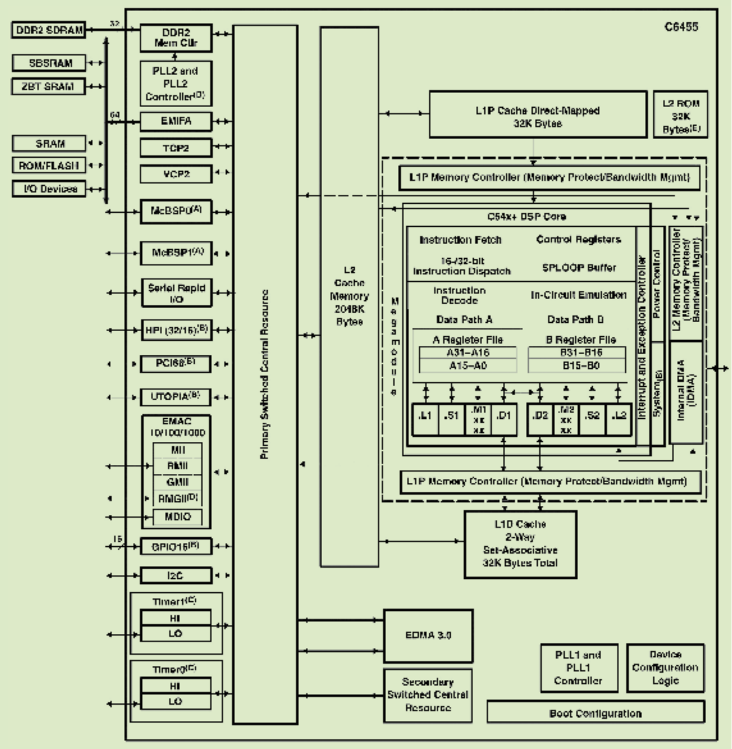

Figure 2

Since different applications may require different system topologies, sRIO is highly flexible in that a system developer can arrange a sRIO-based network in both ring and mesh topologies (Figure 3). Since sRIO uses source routing instead of a broadcast routing approach, only the path between the sender and the receiver in the topology is actually burdened with the transaction. This leaves more bandwidth available in the topology for other DSP devices in the system to communicate with each other concurrently. In addition, multiple processing elements can be connected through a switch, with or without local connections to one another and to ASICs and FPGAs. Multiple processing elements can also be connected in a star topology (five DSPs are all connected to one another in Figure 3).

Lastly, interoperability work is a critical milestone that will help further ease the deployment of RapidIO technology-based systems in applications. The interoperability tests build on the trade association's RapidIO Interconnect Specification Device Interoperability and Compliance Checklists, which was developed as a guide for engineers to develop multi-processing, multi-channel signal-processing solutions. For instance, the first step of device interoperability tests ensures "Device A" is proven to pass a given test with "Device B." sRIO development systems are available so that developers can evaluate and prototype sRIO systems prior to committing to a board design. Thus, all key system elements are available enabling designers to build sRIO systems.

Robert Oshana *is an engineering manager in the Software Development Organization of TI's DSP Systems business. He is responsible for the development of hardware and software debug technology for many of TI's programmable devices. He has 25 years of real-time embedded development experience.*

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Combo JTAG tester for PPC, Pentium, Xscale

Designing complicated FPGA and microprocessor systems inevitably requires testing them. With today's ICs, the permutations of electrical connectivity and software makes the job nearly impossible without sophisticated testing tools such as JTAG boundary scan. ASSET InterTech has teamed up with International Test Technologies (ITT) to create the ScanWorks PCI-200EJ PCI controller card for PowerPCs (and soon for Intel Pentiums and Marvell Xscale CPUs).

Structural faults can be pin-pointed via a JTAG/IEEE 1149.1 boundary scan test, and the onboard programming functions offer a flexibility when coupled with the ScanWorks tool suite. The product also includes microprocessor functional emulation testing, relying on ITT's Master emulation testers. The board's value comes from combining all three types of tests in a single platform, allowing the same GUI and physical connector to the unit under test to simplify a complicated task.

ASSET InterTech
RSC# 31765
www.asset-intertech.com

Low cost PCI Express analyzer

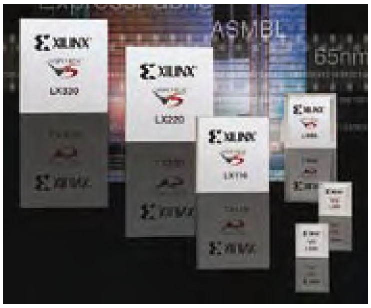
With PCI Express becoming pervasive in embedded systems – including IP cores developed for FPGAs – designers need a way to analyze data moving over the links. The fourth generation PETracer Edge from LeCroy Corporation is based on a card platform that supports x1/x2/x4 lane widths at the full 2.5 Gbits/sec PCIe speeds. The Edge analyzer comes with a comprehensive application tool that's been proven on the company's other analyzer products.

There are powerful triggering, filtering and error reporting capabilities. With PCIe's new protocols, the tool also supports annotated views and charts to assist the user in deciphering traffic and data on the links. Events can be displayed in chronological or logical order, and CRC rechecking assures that the actual data is being displayed, not strange artifacts. In fact, LeCroy feels so strongly about assuring the accuracy of the data being analyzed, that the CRC feature can display decoded data including Transaction Layer Packets (TLPs), Data Link Layer Packets (DLLPs) and all PCI Express primitives. A single mouse click facilitates display and ordering of key information. To save cost, the PRO Edge offers full functionality, while the EXPERT version offers additional deep analysis and bus management troubleshooting and statistics.

LeCroy Corporation
RSC# 31766
www.lecroy.com

Xilinx Virtex-5 family

Shortly before summer Xilinx unveiled the follow-on family to their Virtex-4 series of Platform FPGAs. The Virtex-5 continues the concept of FPGAs earmarked and optimized for certain types of end applications. The company's Advanced Silicon Modular Block (ASMBL) architecture, coupled with on-chip ExpressFabric routing and industry-leading densities sets the new standard for the programmable logic industry. Based upon 65-nm line widths, the family of FPGAs offers 65 percent more capacity and an average of 30 percent speed improvement, with dynamic power consumption reduced by about 35 percent.

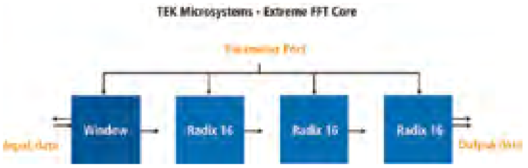


Family members include a Virtex-5 LX for high performance logic, the LXT for serial connectivity, the SXT for DSP with serial connectivity, and the FXT for embedded processing with serial connectivity. The devices are optimized for the so-called market "triple play": convergence of voice, video and data. Key features include: new diagonal interconnects and 6 input LUTs improve on-chip signal interconnects and routing; 550 MHz IP blocks with Clock Management Tile plus PLLs for faster performance and signal processing algorithms; Sparse Chevron packaging allows designers to us up to 1,200 user I/Os and 1.25 Gbits/sec double data rate signals; and increased silicon integration and design techniques provide up to 333,00 logic cells and 1,200 user I/Os. In parallel, Xilinx has and will continue to introduce numerous tools and partnerships to supplant the Virtex-5 devices.

Xilinx
RSC# 30735
www.xilinx.com

Extreme FFT core computes 1M FFTs/sec

In DSP, the benchmark is always the same: how many FFTs can the system perform per unit time. As a secondary criteria, you know the person is serious when the next question involves the resolution (number of points) of the FFT. That's what makes TEK Micro's Extreme FFT Core so whiz-bang: TEK Micro claims that it's 10x faster than any previous implementation, capable of 1 million 4K point FFTs per second. This kind of performance saves SWAP (size, weight and power) in all kinds of systems.

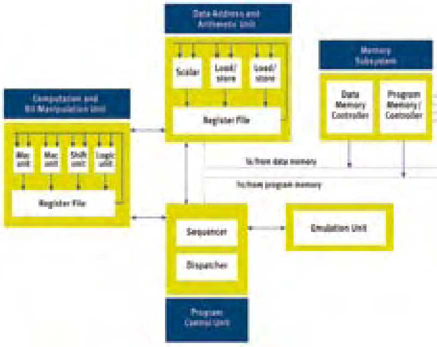


Developed with their European partner QinetiQ (the former British MOD's DERA think tank), the core is pre-integrated with TEK Microsystems' VME VXS-based high-speed serial boards. With a Neptune 2 VXS digitizer card, for example, real-time spectral analysis can be performed at 2.2 GSps. The core is programmable for 1K, 2K and 4K sizes, and uses only about 10,000 programmable logic slices (about 33 percent of a Xilinx VirtexII Pro 70).

TEK Microsystems
RSC# 31767
www.tekmicro.com

3G phone-home DSP core

Handsets and other low footprint devices need max DSP capabilities, but minimum SWAP (size, weight and, power). Satisfying these conflicting goals is the mission of CEVA's CEVA-X1622 fully synthesizable DSP core. The core targets 3G/HSDPA handsets, WiMax terminals, and Smartphones. The low power core offers a configurable memory size of 64 KB or 128 KB, and configurable memory bank organization in 2 or 4 blocks.



The CEVA-X1622 DSP uses an area optimized implementation and On-chip Emulation Module (OCEM) enhancements, making it significantly smaller than other cores such as CEVA's X1620. There is a 16-bit fixed-point dual MAC VLIW architecture with SIMD multimedia operations, up to 8 parallel instructions of either 16- or 32-bit width, and 4 GB of byte-addressable memory space. Video processing and compression are the core's targets, so there are built-in mechanisms and instructions tailored to these kinds of apps. Users can migrate code from the X1620 core to the CEVA-X1622, and also program in C/C++. [Editor's note: CEVA includes the companies previously known as DSP Group, Parthus, and others.]

CEVA **www.ceva-dsp.com**
RSC# 30732

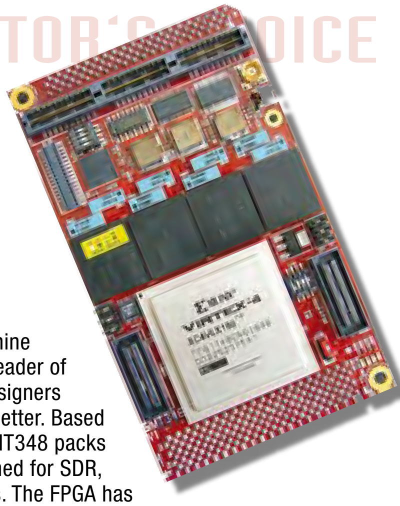
Bend me, shape me

Consumer devices are getting smaller, whether they're portable or designed to sit on a table. Cramming circuitry, displays, human interface and power into small spaces often involves a trick of industrial design origami. This "trick" frequently uses flex circuits to bend wires and sometimes entire PWBs into odd shapes. Manufacturing expert Minco has developed their Flex Circuits Design Kit for engineers who are serious about Gumby-like designs that can reduce space and weight by up to 75 percent. The Design Kit comes with probably the most boring yet most valuable piece of the package: a set of design guidelines honed from years of practical experience.

The guidelines include specifications and manufacturing procedures supported by detailed illustrations with descriptive call-outs and common terms. There's also a sample case holding over 25 actual pieces of raw material and circuit examples. The point of the samples is to educate engineers on "the intrinsic nature of these pieces and how they interact when stacked up". For designers new to flex, there's nothing like a little show and tell to help factor in the parameters of bending, flexing, bend radii, dielectric thickness and type, foil weight, copper plating, number of layers, and number of flexures. Minco's goal with the Design Kit, of course, is to help you choose their service for your first (or next) flex circuit.

Minco **www.minco.com**
RSC# 31768

When is enough DSP power, enough?



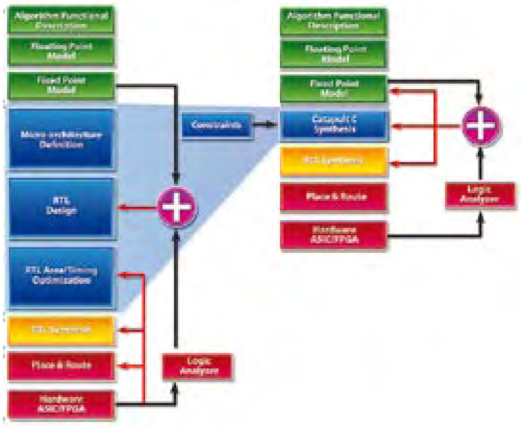
Sundance likens their new DSP mezzanine boards to "Ferraris on steroids." As a reader of Car and Driver, I've seen how smart designers really can make a great product even better. Based upon the Xilinx Virtex-4 LX-160, the SMT348 packs raw speed and scalability and is designed for SDR, WiMax, radar, 3G and other RF systems. The FPGA has direct access to 16 MB of QDRII RAM, and connects to multiple high-speed busses and I/O to keep the data racing in and out of the FPGA.

The base module can be used standalone or connected to other Sundance products including ADC or DAC modules. The Virtex-4 LX is connected to two 60-way SHB connectors for normal LV-TTL interface, or designers can use the Sundance LVDS Bus (SLB) connector with 36 pairs of LVDS to talk to distant equipment.

Sundance Digital Signal Processing **www.sundance.com**
RSC# 31770

Create systems with C++

System synthesis tools are handy for creating, floorplanning, and simulating signal processing systems. Trouble is, most tools use some sort of proprietary "hardware C" that's closely coupled to the target environment. This forces the designer to not only learn the nuances of a new language and tool, but prevents existing system blocks from being easily imported and instantiated. Based on Mentor's already popular Catapult synthesis tool, Catapult SL adds several new features, improves block-level performance, and links to power analysis tools that can aid designers in reducing power consumption by up to 30 percent.



The focus here is on System Level, with the tool's hierarchical design engine coordinating multiple blocks and synthesizing interblock channels and memory buffers. Of course, this is also capable with other tools, but the efficiency and elegance of Catapult SL is achieving success using ANSI C++. The new version also adds carry-save adder, a "design technique for streamlining computations and throughput to increase the performance of individual blocks" when constructing AND, OR and XOR logic. As before, Catapult SL can also create RTL for both ASICs and FPGAs. In all, the tool makes a system designer's job easier while creating more compact designs in ASICs, FPGAs, and other targets.

Mentor Graphics **www.mentor.com**
RSC# 31769

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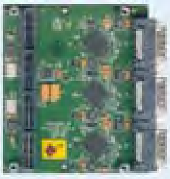

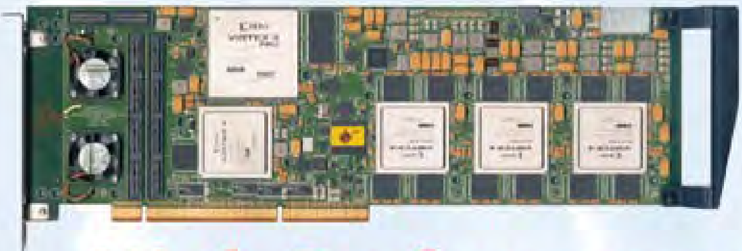

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Photo courtesy of USN

The future of high-performance COTS signal processing

Hybrid FPGA/DSP architecture: the optimal solution

By Jeffry Milrod

Much energy, hype, and column space has been focused on pitting DSP and FPGA-based signal processing solutions against one another. But FPGAs and DSPs are fundamentally different technologies with different strengths and weaknesses and neither one of them can claim outright superiority today. It has becoming increasingly clear that the best approach is a combination of the two technologies, leveraging the strengths of both.

Until recently the basic architectural approach to signal processing COTS products was to put as many DSP chips on a given board format as possible. In the last few years, the same basic approach has been applied with FPGAs in place of programmable DSPs. This approach is simply brute force: use more DSPs or use bigger FPGAs. Subsequently, each new COTS signal processing board generation has become more complex, more expensive (relative to other boards), and more power hungry.

Despite this, application requirements are still outpacing technology improvements – clearly the old paradigms aren't working and a different approach must be developed. Given that both technologies have their place in a signal processing design, this "different approach" needs to be a new hybrid architecture that uses the correct DSP and FPGA technology to solve the correct problem.

Embracing differences

The FPGA vs. DSP debate has been an endless source of discussion in recent times. It may be that FPGAs ultimately obsolete DSPs for high-end applications, or it could be that DSP vendors will provide new price, performance, or power advantages that FPGAs can't compete with. However, we can't predict the future, and in this case it is pointless to try to do so since the two technologies are fundamentally different, each with their own strengths and weaknesses.

It is generally understood that FPGAs are better for high data rates, parallelism, processing densities, and I/O flexibility, while DSPs have advantages in power consumption, ease-of-development, and floating point. FPGAs tend to be better at solving straight forward, well defined, high-speed problems while DSPs are better to implement complicated algorithms that may evolve, involve decision making, or can benefit from the use of floating point.

Most real-world embedded signal processing applications have components that exhibit both of these natures. Therefore, rather than competing these technologies against one another, it is usually better to constructively embrace these differences by leveraging the strengths of both technologies while mitigating their respective weaknesses.

While this has been done for a while at a system level by putting a DSP board in one slot and an FPGA board in another, this loosely coupled approach is *still fundamentally an inelegant brute force technique*, and often induces longer latencies and lowers bandwidths while increasing costs and power consumption.

A better approach to achieve synergy is to embrace the differences by combining both FPGA and DSP compute elements onto one 'hybrid architecture' signal processing card.

Hybrid architecture issues

The concept is simple enough – put DSPs and FPGA together on the same COTS board. However, for this to be truly synergistic and effective, the COTS vendor must carefully navigate a sea of tradeoffs. Major issues including I/O interfacing, interprocessor communication, memory configuration, host interface, control, and an FPGA framework must all be carefully thought out, along with unifying software that makes it all accessible to the user.

I/O interfacing

Given the previously mentioned generally understood advantages of FPGAs, it clearly makes architectural sense to place them close to the signal I/O. In fact, many COTS boards already have FPGAs on them to facilitate I/O reconfigurability. By simply placing the FPGA at the point of data ingress/egress, virtually any data transfer mechanism and/or protocols can be supported, including such diverse methods as PCI, PCI Express, USB, GigE, and Serial RapidIO. This is especially advantageous on newer board formats like VITA 41, VITA 46, and AMC, which support high speed serial, or SerDes communication ports that can implement several different protocols. The FPGA can be reconfigured to allow the board to support a different dot spec and network.

An additional architectural advantage of placing the FPGA at the point of I/O is to facilitate the type of high-speed front-end data reduction, pre-processing problems that FPGAs are so good at solving.

Hybrid architecture optimization issues	
Interface	Host interface
Interprocessor communication (IPC)	Control
Memory configuration	FPGA framework

Inter-Processor Communications (IPC)

Aside from the choice of DSPs and FPGAs themselves, the hybrid architectural issue that most directly impacts signal processing performance is the communication between these compute elements. Obviously, these interfaces must be tightly coupled, low latency, and deterministic. Less obvious is the fact that these IPC should also be much faster in the aggregate than the board's I/O bandwidth. Since the basic idea of hybrid architecture is that the proper type of compute element can be used at the proper place in a given application, the data usually will need to move between several different compute elements – often several times – before it's fully processed.

As shown in Figure 1, data enters the board via the FPGA I/O interface and is optionally pre-processed. Sometimes, as in the case of a down converter or pulse compression algorithm, the pre-processing will reduce the data rates, but a good architecture cannot assume this as many other common pre-processing algorithms, including filters, decoders, and FFTs, don't significantly change the data rate or could even increase it. Therefore, the minimal data bandwidth case is one where the data is sent on to a DSP for additional processing, and then maybe back to the FPGA only for post-processing and output. In this case the IPC data rate only needs to be equal to the I/O data rate. However, in the more general case when the FPGA provides co-processing resources for the DSP, or multiple FPGAs and/or DSPs are required for compute elements, then the IPC data rate requirements can be many times the I/O data rates. For example, if we have a 4x SerDes I/O at 3.125 GHz to the FPGA, this translates to ~1 GBps of external I/O data bandwidth. To support this external I/O, at least 2 GBps of non-blocking data bandwidth is needed between the FPGA and the DSP, with 4 GBps preferable.

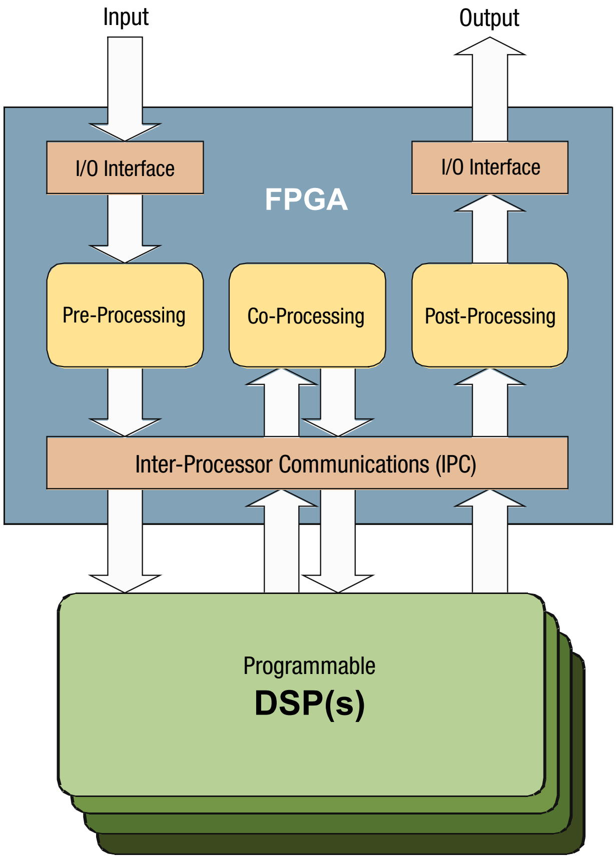

Figure 1

Memory configuration

Not all signal processing applications require bulk memory, but most do. The optimal type, configuration, and even the location of the bulk memory depends on the specific application requirements. Like the I/O interfacing, this is where the inherent flexibility of the FPGA can be leveraged to implement a more versatile COTS board. Connecting modular bulk memory to the FPGA allows many types and configurations of memory to be supported by changing the memory module and reprogramming the FPGA. For example, a 64-bit data bus could be used to support a single 64-bit wide memory bank or reconfigured to support two independent 32-bit banks, possibly even of different types if desired.

Host interface and control

The best processing board in the world is of little value if it can't readily be integrated in to a system. In the COTS world this means standard mechanisms for host interfaces and control, virtually all of which can be support using PCI and/or GigE. The architectural issue then becomes how best to connect these standard interfaces to the COTS board's hybrid compute resources.

One way this can be done is via a *master* board resource that can then command and control the other compute resources via existing IPC; while this approach has the benefit of simplicity, it has downsides including increased control latencies and reducing the effective bandwidth and determinism of the IPC. Another approach could be to implement the standard interfaces on each of the hybrid compute resources directly, but is an ineffective use of resources, would severely limit the selection of DSPs, and doesn't facilitate command and control between the compute elements on the board.

> *It may be that FPGAs ultimately obsolete DSPs for high-end applications, or it could be that DSP vendors will provide new price, performance, or power advantages that FPGAs can't compete with.*

A better way to implement host interface and control on a COTS hybrid signal processing board is by using a bridge from the standard interfaces to a separate command and control bus to each of the FPGAs and DSPs. Since this path is orthogonal to the data paths, the interface to it is often referred to as a control plane (as opposed to the data plane). Having an independent control plane allows the host to directly access and control each resource without impacting data bandwidths. Additionally, the command and control bus can provide a path for the host to directly access the bulk memory on the module, as well as a supplementary method of IPC.

The generic COTS hybrid signal processing architecture shown in Figure 2 shows one way that the previously discussed architectural issues could be handled.

FPGA framework

With infinite possibilities, programming an FPGA can be daunting. This is exacerbated when the FPGA needs to implement

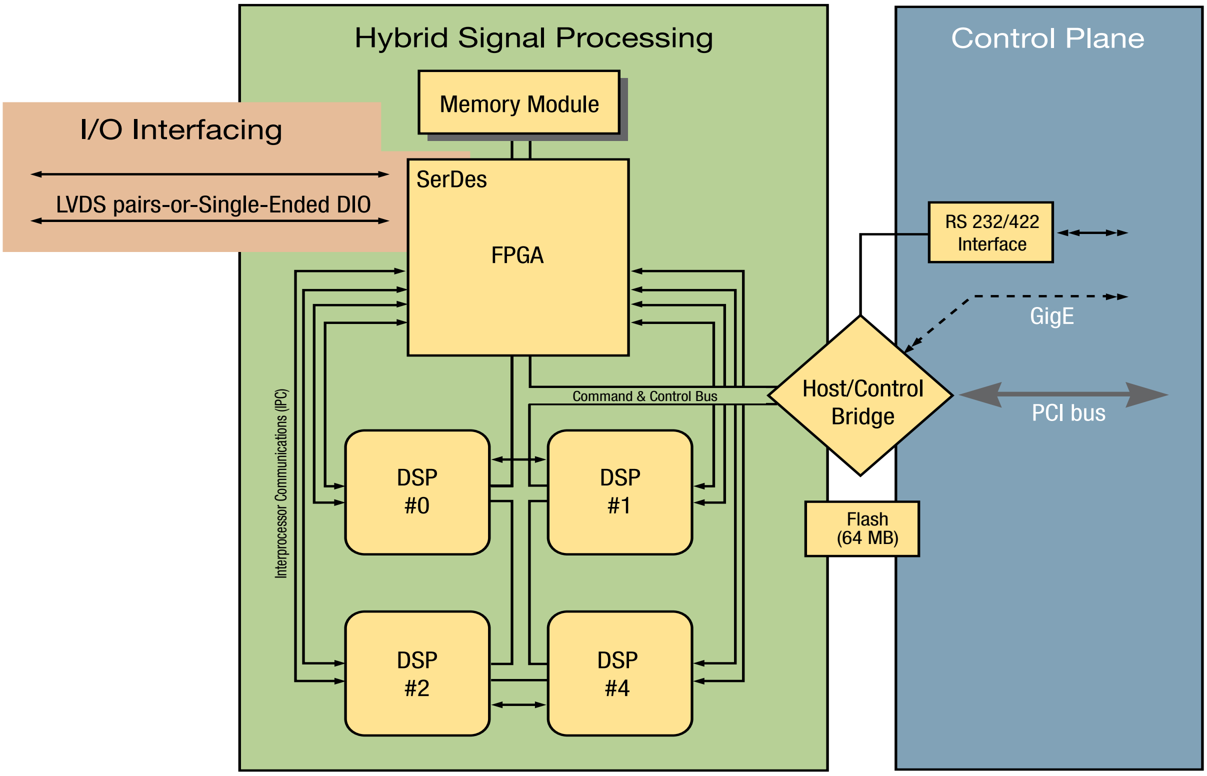

Figure 2

high-performance signal processing and is on a COTS board, with the pin-outs and external interfaces fixed. To reduce these problems, IP modules must, at a minimum, be provided for the board-level hardware interfaces including I/O, memory, IPC, as well as command and control.

Ideally, a complete FPGA framework will also be provided that supports software controlled data routing between the FPGA IP modules, along with documented IP data interfaces that allow the user to develop processing modules that can be inserted into these data flows. In this case, the conceptual data flows shown in Figure 1 can be readily implemented simply by dropping the required pre/co/post-processing blocks (shown in yellow) into the software configurable data flows – at run-time the command and control bus can configure the data flows required for a given application between I/O interfaces, IP processing modules, DSPs, and board-level resources.

Software

The more complex the hardware, the greater the need for low-level software for host interfacing, debug, and run-time command and control. A hybrid architecture has to be more complex than one that is homogeneous; therefore, the need for unifying software is great. For example, even performing a simple board reset now has added complexity: do you want to reboot the DSPs, reconfigure the FPGA, or both?

The challenge to the COTS vendor is to provide software that supports the additional flexibility and complexities – without making it complex to use. Detailed debugging may very well require specialized resources for the different technologies, but the configuration, control, and data of all compute resources must be unified into a single host driver interface library. If an aforementioned FPGA framework is implemented, software must be provided that configures and controls the data routing. Furthermore, the DSPs must have software support for interacting with the FPGA for such things as data transfer, interrupts, coordination, and synchronization; this can be provided via example code, libraries, or better yet, a messaging interface or operating system.

A new solution for traditional COTS

The traditional brute force method of architecting COTS signal processing boards by cramming either more DSPs or more FPGAs in to a slot forces COTS users to choose one set of technical strengths and weaknesses or the other, and has failed to keep up with real-world application demands. Rather than arguing the relative merits of one of these signal processing technologies versus the other while forcing their customers to perform an EXCLUSIVE OR decision, COTS vendors should be offering their customers an AND solution that mitigates the weaknesses and risks of using either technology alone. This is all do-able, and in fact has been done, but it's not easy. While the resulting hybrid signal processing architectures may be initially more difficult to implement, optimize, and make useable, this is exactly the type of heavy-lifting, added value that COTS vendors are supposed to be providing to the COTS users community.

***Jeffry Milrod**, President and CEO of BittWare, Inc., joined BittWare in 1998. He gained extensive design experience at NASA and business experience at Booz, Allen & Hamilton, then merged his technical expertise with his business savvy by starting Ixthos in 1991, which he ran until it was acquired by DY4 Systems in 1997. Jeff holds a BA in Physics from University of Maryland and an MSEE degree from The Johns Hopkins University.*

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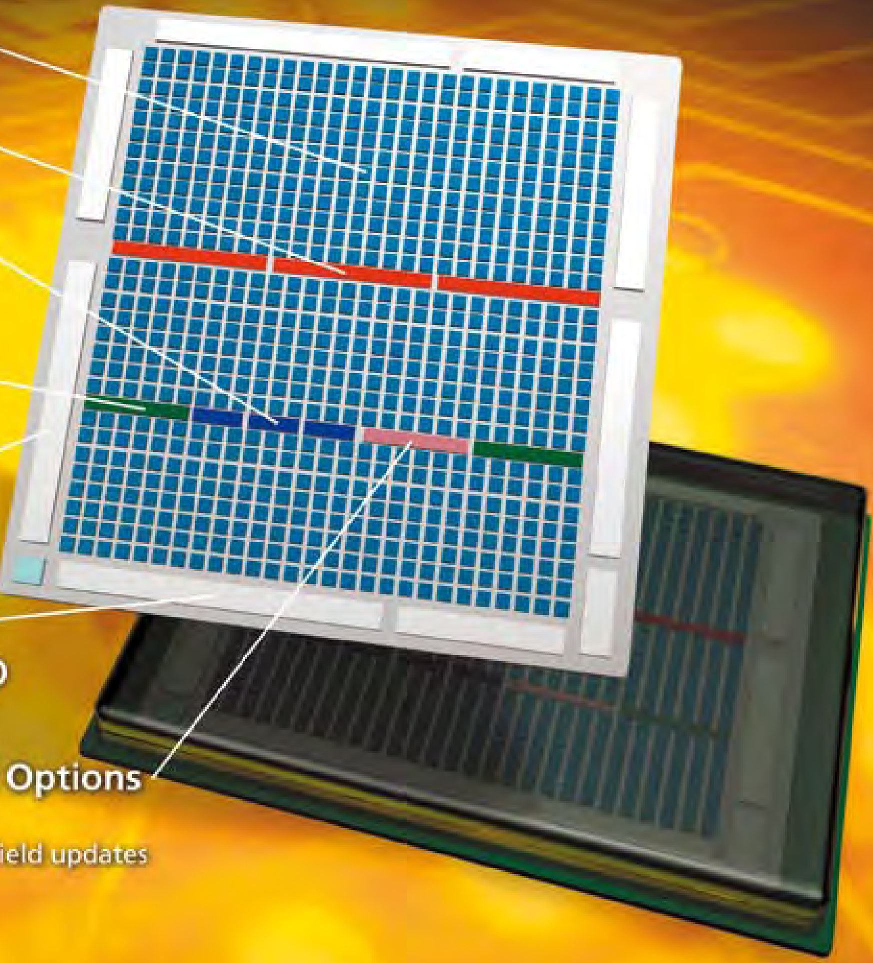

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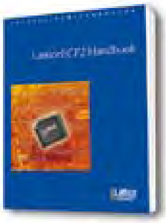

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Using FPGAs to combine multiple digital avionic protocol converters in a single board

By Calmon Cozer

Until now, multiple avionic protocols have required a separate interface board for each protocol. Each additional board adds more components to the system resulting in a higher probability of failure, which translates into a lower system MTBF. Additionally, the resulting system has other disadvantages such as significantly higher prices as well as bigger power requirements. Combining processors with FPGAs yields an excellent and flexible single-board solution to resolve these problems.

Since its introduction in 1992, PC/104 has been the most popular embedded system architecture because of its size, rugged construction, and PC compatibility. Later, for the same reasons CompactPCI also became very popular. There is a premium for size and weight in avionics equipment, making PC/104 and CompactPCI boards very attractive solutions for implementing avionic applications and their communication protocols such as ARINC, MIL-STD-1553, AFDX, and others.

Many highly integrated CPU boards are available on the market for the above mentioned protocols. They include video, graphic processors, hard drives, and many other types of controllers. However, few of these manufacturers have also implemented embedded digital avionic I/O and protocols. The reason for this may stem from the fact that avionics is too limited a market to justify development of such a board.

Elsewhere in the market, there are a variety of digital protocols for civil and military applications. However, they are not all compatible, having different transfer data rates, different data frames, and different architectures. Typically, a user selects the appropriate board for each protocol, and a system with multiple digital communication protocols requires multiple interface boards. This may resolve the problem in a limited sense, but affect other issues by creating major limitations in cases where there is no physical space for system upgrades. What's ideally needed is a programmable PC/104 or CompactPCI board that can realize multiple avionics interfaces and protocols.

Avionic protocols

The most popular protocol used in civil aircraft is ARINC 429. It operates at two baud rates: 12.5 KHz or 100 KHz. It is point to point and has a differential NRZI 10 Vpp signal with a 32 bit word data structure. For the military, the most common digital communication protocol is known as MIL-STD-1553. It operates as a network with a master (bus controller or BC) and slaves (remote terminal or RT), has a data transfer rate of 1 MHz using a 20-bit word data structure with maximum 33 words in each frame, which is transferred through a transformer coupling. Figure 1 shows the data bit structure for a BC command word, including bit definitions and bus transmission order (in *bit time*).

1553 Command Word Structure

Command Word

	MSB				LSB		MSB				LSB	MSB				LSB
Bit Time	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value						0/1										
Description	RT Address					R/T	Sub-Address					Word Count				

RT Address: defines which terminal will receive a command
R/T: shows when set to zero, logic Terminal receives data; when set to 1 Terminal transmits data
Sub-Address: the sub-system under required terminal
Word Count: the number of words following the BC command or RT data answer

Figure 1

The new protocol AFDX or ARINC 664, implemented in new airplanes such as the Airbus 380 and Boeing 787, operates at 10 or 100 MHz, uses *Manchester* encoding and decoding. Access control is similar to Ethernet and gained via Carrier Sense, Multiple Access with Collision Detect (*CSMA/CD*). AFDX's data structure is shown in Figure 2.

Programmablility needs more than microcontrollers

Many of today's microcontrollers offer an impressive combination of integrated features and interfaces, including hardware-based ADCs and DACs, PWM support and a range of serial and parallel interfaces. Popular microcontrollers like the 80C196 from Intel provide high speed I/O and watchdog timer functionality. The primary limitations of these devices are the quantity and quality of the available interfaces and, of course, most microcontrollers are not field programmable like the 80C196. Instead, they are oriented to the most popular protocols like the asynchronous protocol of the on-board UART and they usually transmit at a slower rate. Another limitation is the microcontroller's speed, which is normally less than 10 MIPS, making it impossible to handle a per bit single serial fast protocol above 1 MHz.

Microcontrollers are sequential machines and are incapable of simultaneously translating serial to parallel data while storing incoming multiple data. They are also too slow to meet the exacting standards of avionic protocols. The interrupt time required to read data from the internal serial to parallel register, store the data into internal or external memory, set flags, increment pointers and verify multiple conditions (like end of buffer) typically takes *hundreds* of instruction cycles.

The problem arises because MCUs need to handle their multiple on-board UARTS, but as channels are added to a board, the MCU's ability to handle the data transfer lessens. For example, if an instruction cycle executes in 500 nanoseconds, and it takes 200 instruction cycles to read and store information, the processor will be busy for 100 microseconds. This time is equivalent to 5 incoming words from MIL-STD-1553, or 500 words from an AFDX bus line. Clearly a microcontroller alone can't help us create a single board, multi-protocol avionics I/O solution.

System solution

We have found that an FPGA chip with dedicated logic and memory capabilities can resolve many of these problems. When coupled with the appropriate microcontroller, the combination of MCU plus FPGA can not only process and analyze data, but provide the versatility to support multiple protocols while often increasing the number of system channels.

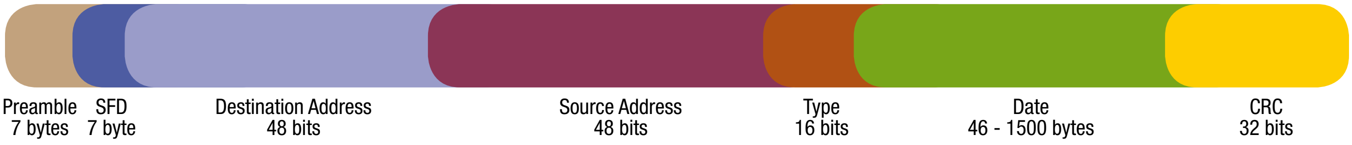
The combination of a CPU with a FPGA chip gives a very flexible system solution; the CPU has the operational code to analyze and process data while the FPGA is used for I/O operation. Most FPGAs require an external non-volatile storage memory device to hold the device configuration storage. Following power-up, the FPGA configures itself by downloading the configuration from non-volatile memory. Often the download is serial and may take hundreds of milliseconds for the download operation to complete. To resolve this and other issues, flash-based programmable microcontrollers can be used to facilitate loading the FPGA and storing the serial programming bit stream.

There are a number of advantages for using a flash microcontroller embedded with the system code and the FPGA configuration**.** They include: relying on only one device to reprogram for any modification; the FPGA download configuration is done in parallel mode via the CPU bus, taking a fraction of the time of a serial download (external PROM); the number of components in the system is reduced, increasing the MTBF, decreasing physical size and significantly cutting board cost; and the CPU can be programmed through a standard RS-232 PC connection. In this way, the board can be upgraded with a new software version without removing any portion of the installed equipment. One additional advantage is that the board can increase the number of avionic serial channels (for example: ARINC, MIL-STD-1553, and so on) as long as the hardware interface is available.

Regarding programming the CPU via an RS-232 connection, this is a very important issue when dealing with avionic applications. Whenever equipment is removed from an aircraft, it must pass through an extensive set of tests before it can be reinstalled. A field programmable unit avoids the inconvenience (time and money) of a reinstall. When the equipment can be easily reprogrammed via a serial connection hooked to a PC, the elegance of the design is realized. Figure 3 shows the MCU/FPGA combination, including the various system interfaces. In this block diagram, a Xilinx FPGA is shown. The requirements for FPGA selection are listed in Table 1.

Example system: Universal Avionic Design Interface

The UADI is an intelligent interface, incorporating all of the above features and functionality into its implementation and realizing the logic shown in Figure 3. It uses a RISC-based Texas Instruments MSP430 microcontroller. This chip runs



Preamble Field: A 7 bit pattern of alternating ones and zeros which are used to synchronize the receiver clock to the incoming data packet.

Start Frame Delimiter (SFD): indicates the beginning of the frame; [10101011].

Destination Address: The first bit (MSB) distinguishes between an individual or group address. The second bit distinguishes between locally or globally administered addresses.

Source Address: The first bit (MSB) is reserved and set to zero. The second bit distinguishes between locally or globally administrated addresses.

Length/Frame Type: The field has two meanings: if the value is <1536 decimal, it indicates the number of the logical link control in the data field; if is ≥1536 decimal the number indicates the client protocol.

Data: user data (payload).

CRC: an algorithm is used during transmit and receive to generate cyclic redundancy check values.

Figure 2

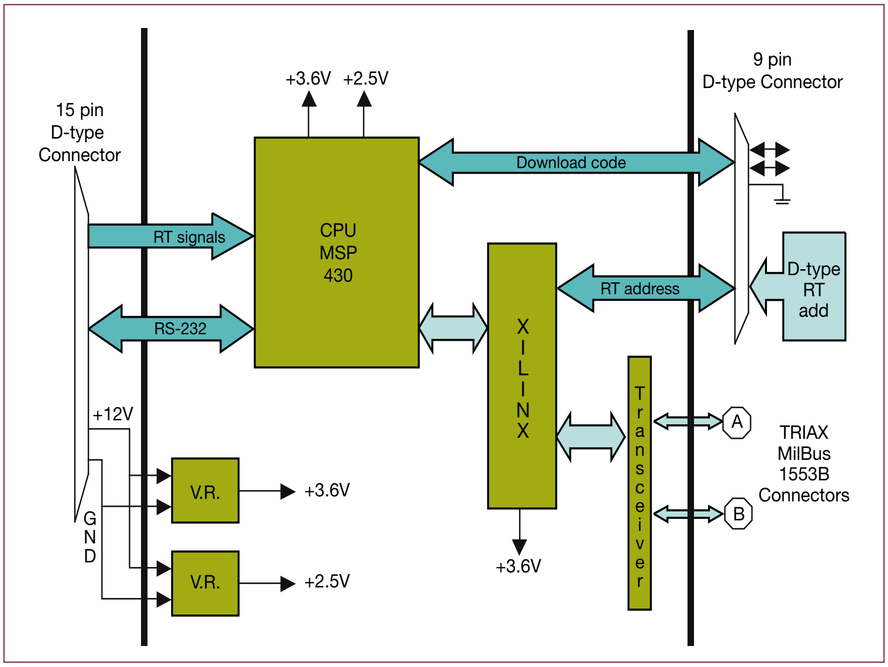


Figure 3

> *When coupled with the appropriate microcontroller, the combination of MCU plus FPGA can not only process and analyze data, but provide the versatility to support multiple protocols.*

on extremely low power – less than 10 mA during operation in the micro-Ampere range during stand-by. It combines two asynchronous serial ports, eight 12-bit ADCs, multiple general I/O, PWM, and timers with an average instruction cycle of 4 MIPS.

The FPGA selected is part of the Xilinx's Spartan II family, combining all the features defined in the above sections. The FPGA design includes various modules, which manage multiple protocols and/or channels. It takes advantage of the architecture flexibility to include a variety of functions, giving the user an extremely powerful tool.

The UADI combines a variety of ARINC protocols, MIL-STD-1553, and RS-232/422. Currently, AFDX is being tested and we expect to have it fully operating before the end of this year. This basic functionality can easily be implemented on PCI, 3U CompactPCI (Figure 4), PC/104, PMC, and on a general purpose SBC. All can be based on the same CPU firmware that includes FPGA software initialization and operational code. The simplicity of theses boards creates a powerful low power interface with minimum components and a very high MTBF.

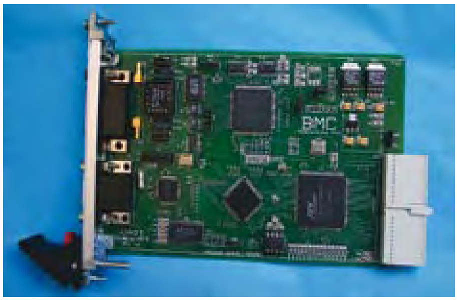


Figure 4

Calmon Cozer is the Director of Engineering for BMC Communications Corp. He is responsible for all avionic interface products. He has serviced the military and aerospace industry for the past 20 years. Mr. Cozer has a BS in Electrical Engineering from The Israel Institute of Technology and a MA in Computer Science from Queens College, NY.

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Software programmable	
Density	The density must be large enough to combine all necessary logic capable of supporting multiple protocols. Each protocol design module requires logic which can vary from 50 to 300 internal slices. As more slices have the selected device, more protocol modules can be implemented under the same design.
Memory	Memory is used for store incoming data and as dual port memory for mailboxes between the host computer and board interface. FPGA memory cell size can vary between 1K word and 100K words. The selection should be made according to application requirements.
Ample I/O	Additional I/O pin signals, capable of interfacing with TTL 5V or 3.3V logic level. This option provides the programmer with the capability to add logic signals for future system upgrades.
Low power	Since we're replacing multiple boards with a single board, the FPGA must not consume our "saved" power.
>200 MHz	Choose a minimum internal frequency of 200 MHz, which provides the speed to handle the new faster avionic protocols like AFDX (running at a data transfer speed of 100 MHz).

Table 1

ar·chi·tect (är'kĭ-tĕkt') n.
One that plans or devises

build·er (bĭl'dər) n.
One that builds

ge·dae (jē-dā) n.
architect *and* builder

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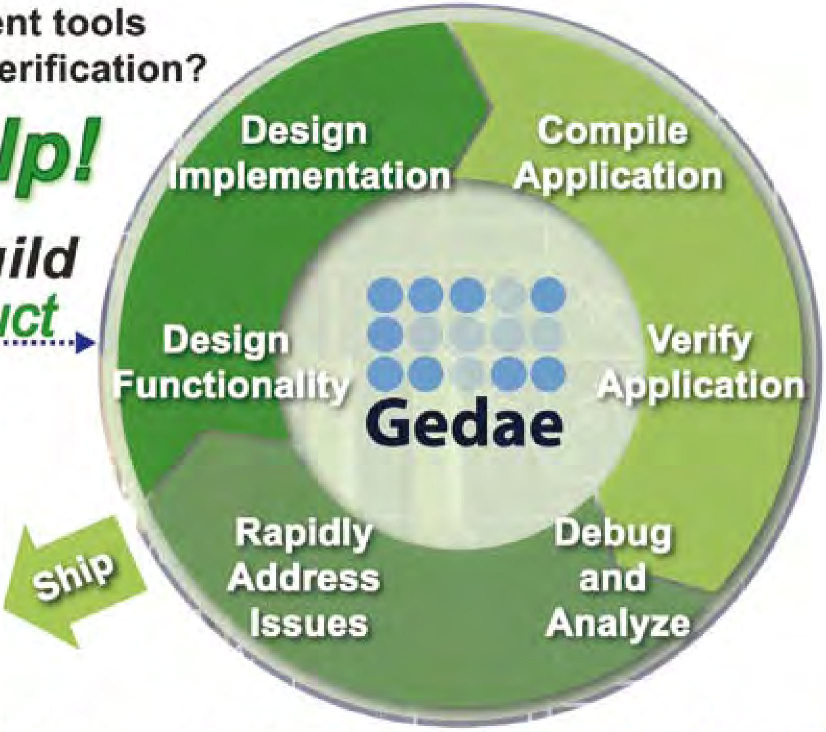

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COTS digital radio receiver system is *good to go*

By Daniel McLane, Amit Mane, and Billy Kao

This software-defined radio reference design implements a 40-channel digital receiver system that integrates reprogrammable FPGAs with high-speed DSPs to deliver 1 GHz data rates in 10 kHz frequency increments. The hardware-in-the loop design methodology allows the developer to design and download a whole system to hardware in hours. Each design iteration can be implemented and tested in less than a day.

In the competitive business world of the quick and the dead, a commercial-off-the-shelf (COTS) design solution can give a software-defined radio (SDR) designer a significant time-to-market advantage. Designing a digital radio receiver (DRR) system from the board up would not only be unacceptably time-consuming, it would also be prohibitively expensive in terms of non-recurring engineering (NRE) costs.

This paper demonstrates a HW/SW COTS reference design package for a high-performance SDR DRR system using new design tools and hardware that can dramatically reduce the complexity and development time to bring a product to market on a mission-critical timeline.

System description

The DRR reference design implements a 40-channel digital receiver on a single 6U CompactPCI card set. The DRR system integrates the reprogrammable flexibility and computing power of Xilinx Virtex-II Pro XC2VP40 FPGAs with high-speed Texas Instruments (TI) TMS320C6416 DSPs to provide a fully programmable SDR system.

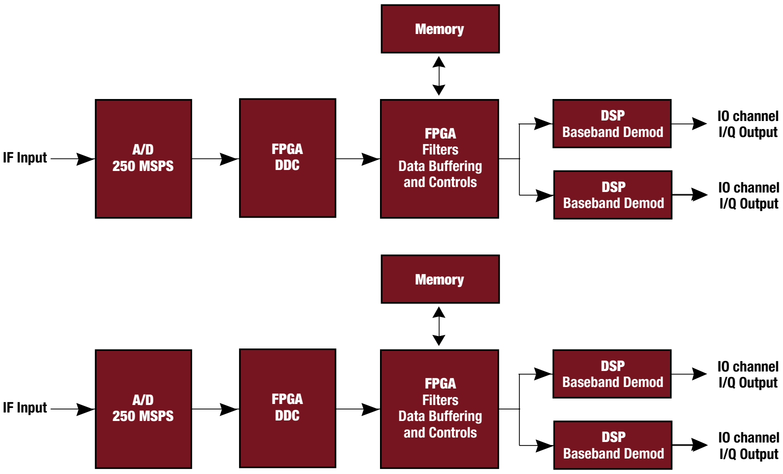

Figure 1

The V-II Pro FPGAs each have four IBM PowerPC embedded processors that, combined with the 1 GHz TI DSPs, provide a powerful and flexible computing core, allowing all of the signal processing to be implemented in software.

The system block diagram in Figure 1 shows the major hardware features from the signal digitizers through the signal processing FPGAs and into the DSPs.

Signal path

The DRR signal processing starts with a wideband, intermediate frequency (IF) Linear Technology LTC2245 signal digitizer capable of up to 250 MSps. The 12-bit analog-to-digital device has a 350 MHz analog input bandwidth suitable for a wide range of IF signal sampling and under-sampling applications. The IF signal digitizing is followed by a digital down converter (DDC) and then channel filters. The down converted channel signal is subsequently filtered into baseband channel data, ready for demodulation by the DSPs.

The Mathworks' MATLAB Simulink design tool allows the developer to implement a block diagram directly into the logic hardware. MATLAB uses Xilinx System Generator software to create an FPGA signal processing design, and then the DRR reference design hardware board support package (BSP) enables the implementation straight from the MATLAB program to hardware.

Using the DRR reference design, the DRR signal processing can be customized for multiple applications including high-end coprocessing, wireless communications, video, biometrics, and electronic warfare.

Real-time simulation saves time

In the MATLAB Simulink environment using the Xilinx System Generator blockset, the simulation data is bit-true, cycle-true, and accurately reflects the performance of the real system. Characteristics of a system can be easily modified by changing the parameters in the blocksets and then immediately verified in real-time simulation in hardware.

Hardware interfaces and supporting features in the FPGAs – such as system controls, DSP interface, and data buffering – are provided as HDL code into which the signal processing is integrated. The TI DSP real-time operating system (RTOS) provides device drivers for the DSP that allow the SDR developer to concentrate efforts on application-specific signal processing.

Hardware-in-the-loop

The entire SDR signal-processing model for the DDC and channel filtering is built using Xilinx System Generator under the MATLAB Simulink environment. This is a key feature for rapid DRR development, because the designer can use MATLAB as part of the system verification. This hardware-in-the-loop methodology means the MATLAB model can run in real-time in hardware and immediately be evaluated against the theoretical performance.

This is an extremely powerful method of code development, because it bridges the gap between the whiteboard concept and the hardware. The whole DRR system can be designed and downloaded to the hardware in hours. Each design iteration only takes hours, not days, to implement and test.

Digital down converter and filters

The initial signal processing step in the DRR system is digital down conversion. The DDC first mixes the digitized IF signal with a tuning signal resulting in a frequency shift to the baseband represented as an in-phase and quadrature (I/Q) data pair for the channel. The I/Q signals are then filtered and decimated using a cascaded integrator-comb (CIC) filter.

The CIC filter allows the FPGA to process the data at rates of up to 208 MSps from the digitizer. The CIC filter is followed by compensation (CFIR) and programmable (PFIR) filters built in another FPGA. These filters reject out-of-band noise and provide channel isolation after the digital down conversion.

The end-to end system data is decimated by a factor of 120 in the DRR reference design. This decimation results in channel data at 1.083 MSps for each channel.

Filter design

During the filter design process, the designer trades off the competing demands of achieving better channel separation by using a sharper filter with higher out-of-band rejection against the size and complexity of the filters. Filters with high data rates and large numbers of poles require more logic resources to implement. Therefore, the filter designs are a critical factor in meeting the system channel separation requirements, while still keeping the design practical.

This design process is made much easier because trade-offs can be determined during the design stage with the assurance that the system behavior will match the theoretical model created in the Xilinx System Generator software.

Once the DDC and system filters are designed using the MATLAB system model, the designer can simulate the entire DRR process and verify functionality using bit-true and cycle-true modeling of the hardware. The reliability of the modeling allows the designer to fine-tune the system performance to meet the most exacting requirements.

Hardware

The IF signal is digitized using Linear Technology A/D devices mounted on two ultra-wide (UWB) PMC modules. After the signal undergoes digital down conversion and initial filtering in a Virtex-II Pro FPGA on the UWB module, the signal is transmitted to a Quadia CompactPCI board for baseband processing by two more Virtex-II Pro FPGAS and four TI DSPs. Each DSP processes 10 discrete channels. The Quadia board is shown in Figure 2.

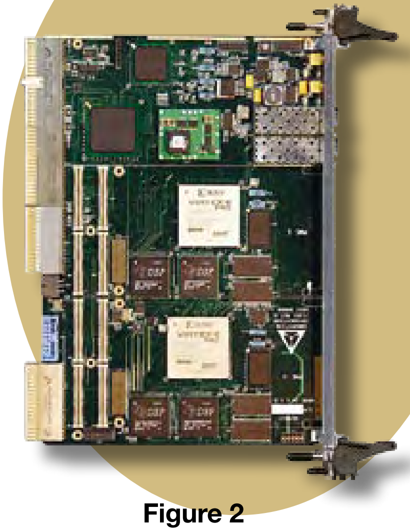

Figure 2

The host computer controls the DRR system initialization, tuning frequency, CIC filter gain, and spectral inversion. Configuring the DRR channel features directly from the host PCI bus saves time, because these functions do not have to be recompiled in the logic.

The system allows all channels to trigger simultaneously and to operate synchronously. Data buffering in the DRR for each DSP helps to meet the real-time demands on the system for processing. The data buffering implements a 16 MB queue for each DSP in external DDR DRAM.

The DRR logic consumes about 90 percent of each UWB FPGA and 50 percent of each Quadia FPGA. The TI DSP chips are virtually 100 percent available for baseband processing and analysis.

DRR in operation

Figure 3 charts captured I/Q data for the 10 channels delivered to one DSP for a 97.5 MHz IF signal under-sampled at 130 MSps. The frequency of the input sine wave is 97.5 MHz, and the tuning frequency for each of the 10 channels ranges from 32.51 MHz to 32.60 MHz in 10 kHz increments.

The Figure 3 results match the MATLAB theoretical model for frequency response and performance. Ultimately, the DRR system is only limited in its performance by the design of the digitizing hardware.

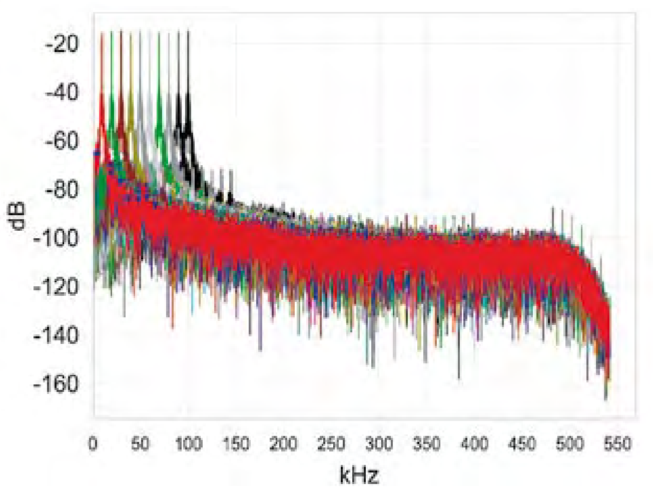

Figure 3

DRR host and DSP software

The DSP software, running under TI's DSP RTOS is responsible for the baseband signal processing and data flow to the host. The host software, running under Windows, is used for DRR configuration, data logging, and system monitoring.

The DRR reference design provides C++ development libraries on both the host and the target DSPs to perform the management of the hardware and data flow. The DRR system can capture and deliver snapshots of data to disk on command from the host. The application then logs the data to disk for analysis.

Conclusion

By taking advantage of a high-performance COTS reference design such as the DRR described in this paper, the SDR designer can be a winner in the race to be first-to-market.

The DRR system was developed by Innovative Integration Inc. of Simi Valley, Calif., USA. The company specializes in DSP-based signal processing and hardware-assisted (FPGA) signal processing, as well as real-time systems and PC-based real-time data acquisition.

Offered as a total COTS package, the DRR reference design package has all the hardware and software – including the MATLAB board support packet and proprietary libraries – a designer needs to implement a customized, high-performance SDR receiver system. For more information, please visit www.innovative-dsp.com/DRR.

***Daniel McLane** co-founded Innovative Integration in 1990, and leads the hardware and signal processing engineering teams. He is a key designer for Innovative Integration and has designed electronics and embedded systems for signal processing, controls, and data acquisition for more than 20 years. Dan holds a BSME degree from Purdue University and an MSME from the University of California at Los Angeles (UCLA). Daniel can be reached at dmclane@innovative-dsp.com.*

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ISSN: Print 1524-9212
Publication Agreement Number: 40048627
Canada return address: WDS, Station A, PO Box 54, Windsor, ON N9A 615

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Mid-Tex Cellular deploys real world SDR

An interview with Toney Prather, visionary and part-time humorist

EDITOR'S NOTE

With this year's 2006 Software Defined Radio Forum just around the corner, we thought it would be an interesting retrospective to look at last year's *SDRF keynote speech. Executive Toney Prather shared the stage with a number of deep, technical briefings and used Texas humor to woo the crowd from the entirely theoretical, to his company's hugely successful deployed SDR equipment. Mid-Tex services a rural area with entrenched competitors such as Sprint, Verizon, T Mobile, Nextel, (now owned by Sprint) and Cingular. Their strategy is to easily roll out new services such as picture phones, reality TV voting, and concierge-type services.*

Mid-Tex Cellular is using SDR in their basestation, using software developed by Vanu, Inc. Mid-Tex Cellular is overlaying its existing TDMA-based wireless network with a new GSM/GPRS-based system using HP servers and Vanu software.

Editor Chris Ciufo sat down with Toney Prather in Anaheim, CA.

DSP: ***First of all thank you very much for the entertainment this morning, it was very enjoyable. Tell us about Mid-Tex Cellular.***

PRATHER: I looked at the speaker yesterday and the speaker tomorrow and I wondered "What the heck am I doing here?" And I decided … these are the smart guys and I'm the entertainment between. As for the company, we're locally owned by two small wireline telcos and we provide wireless services to customers in six counties over 8,000 square miles right in the middle of Texas.

Our SDR solution is designed to extend our coverage and distribute capacity to where it's needed. And since we're small, the equipment needs to be flexible and cost-effective. The best thing about SDR is that we can deploy new services quickly and efficiently.

DSP: ***I understand you've been using Vanu's COTS SDR reconfigurable equipment for quite a while. During your keynote you talked about easily adding new services to your network to support legacy customers, such as iDen and TDMA. How does it work?***

PRATHER: We are purely GSM today. I would say three, three and a half years ago we started all this because we wanted to add TDMA to our system as those old cell sites died, but we decided we'd never be able to add TDMA [to the rest of our system] due to the radio, because they tell me that would be *simple switching*. There's no such thing as an "off switch" TDMA.

We've given up on that idea, so what we'll have to do is when we get to about the 2/3 penetration point on our customer base [switching to GSM] we're just going to have to wholesale them over to it. And I know that's going to be ugly when it happens because you know, we're talking about some farmers that are holding on to analog bag phones in their tractor because it works.

DSP: ***Do you know of any other cellular carriers like yourself who are using software defined radio in a cellular environment?***

PRATHER: Vanu has two more orders that are in process. We're actually involved in doing switching for one of them, and you'd have to talk to Vanu.

DSP: ***Do you think that it would be possible to use your system and SDR to start relaying other radio systems, such as TDMA as you mentioned?***

PRATHER: It would, but we're dealing with a frequency issue and the equipment's RF capability. As well, other people are working on making an RF unit that has a wider bandwidth. That technology is going to come along first, and while people will tell you they're doing that, they're doing it in small areas. I mean now let's get it to where it can reach ten miles. That's a big jump from where we are today, so it's a great idea and it'll be there someday, but I don't have a timeline. You know, it's just a *technology issue* for the RF people.

DSP: ***What other services do you think you could easily add to your SDR set-up?***

PRATHER: I think we'll leave out the ability to have one system that works GSM and CDMA together because they're on different frequencies. Yet we *could* run CDMA and GSM similar frequencies as just carrier selections. You could run them in parallel on the cell site, and in effect have twenty carriers. Because it's just an application, phones come up and say "I need to use your service, whatever it is". It may be that the only way you could do it today is build a GSM and a CDMA side by side, with no sharing of spectrum.

This way all the customer's phones will work. If I've got twenty "lines" available, I can have 20 GSM or 20 CDMA, or I can have 15 and 5, or 10 and 10 because everytime the phone comes up it just looks and says "Oh you're a CDMA phone, you need this. Here's the application stuck on this channel, on this frequency set." So you've actually built one network that looks like two.

INTERVIEW

Shatter Processing Limits in Your Wireless Applications

Breakout performance from BittWare's New DSP Advanced Mezzanine Card (AdvancedMC™)

Combining the best-in-class performance of Analog Devices TigerSHARC with the benefits of AdvancedMC, the B2-AMC is ready for your wireless applications: 2G, 2.5G, 3G, WiMAX, and Software Defined Radio. Using the superscalar architecture of the ADSP-TS201 TigerSHARC DSPs, the B2-AMC provides an unprecedented 14.4 GFLOPs and 57.5 GOPS of processing power. A large Altera Stratix II FPGA implements BittWare's ATLANTiS architecture, seamlessly integrating the DSP processing power with your switch fabric of choice: Serial RapidIO™, PCI Express™, Advanced Switching Interconnect, GigE, or XAUI™ (10 GigE). In addition to the multiprocessor scalability of the TigerSHARC, the board features a variety of front and back panel I/O interfaces, an IPMI system management interface, and system synchronization via AMC system clocks. Ideal for use in AdvancedTCA®, MicroTCA, or custom systems, the B2-AMC will give your wireless application the power it needs.

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DSP: ***What about future plans and applications?***

PRATHER: It's all in the same bandwidth, [using] services as applications. For instance, we didn't have GPRS when I first started, no one had to visit the cell sites to install it. But we added it – it was just a software download.

DSP: ***Do you know of other carriers – such as the big nationwide telcos – who are doing anything like this?***

PRATHER: Most of them have visited my system. We were just the testbed. I saw it in operation in the lab for it to really work, you've got to get out in the real world and see what it does. So we tried it and played with it a lot for a good period of time and decided it was going to work for our 13,000 customers. Initially, we put handsets in employees' hands and told them to use them. I guess we had the thing up probably about seven or eight months before we turned it loose to the public in March [of 2005].

We've now moved 2,800 customers onto this system, and they are unaware of this, because it just doesn't matter to them. It's the same old off-the-shelf handset; there's nothing special. It's a GSM handset.

From a business standpoint, maybe we are off on a little *early adopter ledge*. I understand the big carriers have their processes they have to go through, and maybe they can't be early adopters. But I know they're all looking at [SDR] and working with it – they just have to decide when to do it. DSP-FPGA.com

Toney Prather *is Vice-President of First American Communications Enterprise, Inc. (FACE), and President of all of FACE's nine subsidiaries. He has been employed by a FACE subsidiary, Comanche County Telephone Co., Inc. since 1979 and prior to that time was employed by Great Southwest Telephone Corp. Mr. Prather serves as Managing General Partner for Mid-Tex Cellular, Ltd., in which a FACE subsidiary owns controlling interest. He oversees all aspects of the various FACE subsidiaries, which has 100 employees, provides telecommunications services to over 29,000 customers.*

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The benefits of FPGA coprocessing

By Tom Hill

The Xilinx ESL Initiative brings the horsepower of an FPGA coprocessor closer to the reach of traditional DSP system designers.

High-performance DSP platforms, traditionally based on general-purpose DSP processors running algorithms developed in C, have been migrating towards the use of an FPGA preprocessor or coprocessor. Doing so can provide significant performance, power, and cost advantages (see Figure 1).

Even with these considerable advantages, design teams accustomed to working on processor-based systems may avoid using FPGAs because they lack the hardware skills necessary to use one as a coprocessor. Unfamiliarity with traditional hardware design methodologies such as VHDL and Verilog limits or prevents the using an FPGA, oftentimes resulting in more expensive and power-hungry designs. In this issue, Tom explains how a new group of emerging design tools called ESL (electronic system level) promises to address this methodology issue, allowing processor-based developers to accelerate their designs with programmable logic while maintaining a common design methodology for hardware and software.

Boosting performance with FPGA coprocessing

Designers can realize significant improvements in the performance of a DSP system by taking advantage of the flexibility of the FPGA fabric for operations benefiting from parallelism. Common examples include (but are not limited to) FIR filtering, FFTs, digital down conversion, and forward error correction (FEC) blocks. Xilinx Virtex-4 and Virtex-5 architectures provide as many as 512 parallel multipliers capable of running in excess of 500 MHz to provide a peak DSP performance of 256 GMACs. By offloading operations that require high-speed parallel processing onto the FPGA and leaving operations that require high-speed serial processing on the DSP, the performance and cost of the DSP system are optimized while lowering system power requirements.

But FPGA embedded processing can also lower costs. A DSP hardware system that includes an FPGA coprocessor offers numerous implementation options for the operations contained within the C algorithm, such as partitioning the algorithm between the DSP processor, the

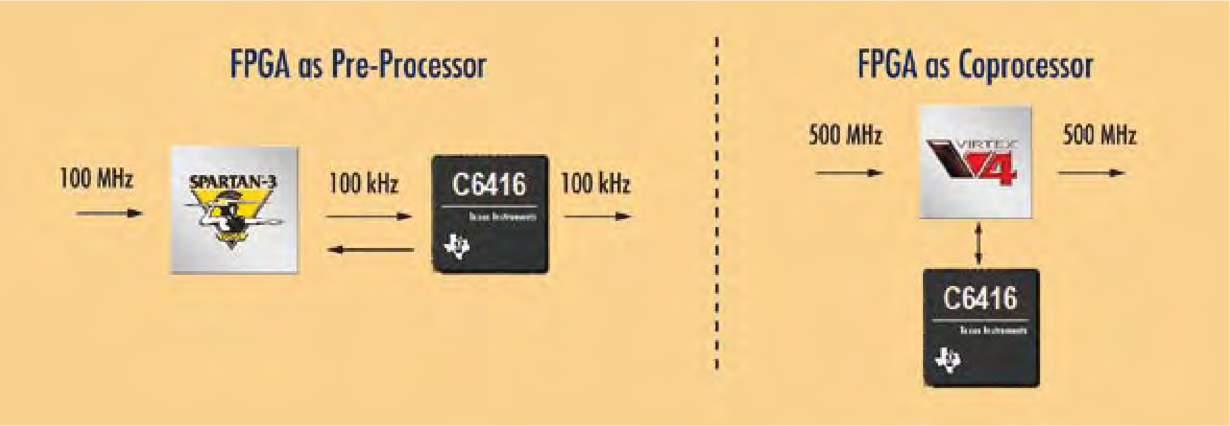

Figure 1

FPGA-configurable logic blocks (CLBs), and the FPGA embedded processor. The Virtex-4 device offers two types of embedded processors: the MicroBlaze soft-core processor, often used for system control, and the higher performance PowerPC hard-core embedded processor. Parallel operations partitioned into the FPGA fabric can be used directly in a DSP datapath or configured as a hardware accelerator to one of these embedded processors.

The challenge facing designers is how to partition DSP system operations into the available hardware resources in the most efficient and cost-effective manner. How best to use FPGA embedded processors is not always obvious, but this hardware resource can have the greatest impact on lowering overall system cost. FPGA embedded processors provide an opportunity to consolidate all noncritical operations into software running on the embedded processors, minimizing the total amount of hardware resources required for the system.

From C to gates

When targeting an FPGA, the term *C to gates* refers to a C-synthesis design flow that creates one of two implementation options – direct implementation onto the FPGA fabric as a DSP module, or the creation of a hardware accelerator for use with the MicroBlaze or PowerPC 405 embedded processor (shown in Figure 2). When an operation lies directly in the DSP datapath, the highest performance is achieved by implementing an operation as a DSP module. This involves synthesizing the C code directly into RTL and then instantiating the block into the DSP datapath. Designers can perform this instantiation using traditional HDL design methodologies or through system-level design tools such as System Generator for DSP. Through direct instantiation, the highest performance can be achieved with minimal overhead.

The leading C-synthesis tools are capable of delivering performance approaching that of hand-coded RTL – but achieving this requires detailed knowledge of C-synthesis tool operation and coding styles. Code modifications and the addition of in-line synthesis instructions for inserting parallelism and pipeline stages are typically required to achieve the desired performance. Even with these modifications, however, the productivity gains can be significant. The C-system model remains the golden source driving the design flow.

An alternative and often simpler approach is to create a hardware accelerator for one of the Xilinx embedded processors. The processor remains the primary target for the C routines, with the exception that performance-critical operations are pushed to the FPGA logic in the form of a hardware accelerator. This provides a more software-centric design methodology. However, some performance is sacrificed with this approach. C routines are synthesized to RTL, similar to the DSP module approach, except that the top-level entity is wrapped with interface logic to allow it to connect to one of the Xilinx embedded processor buses. This creates a hardware accelerator that can be imported into the Xilinx EDK environment and called through a software-friendly C function call.

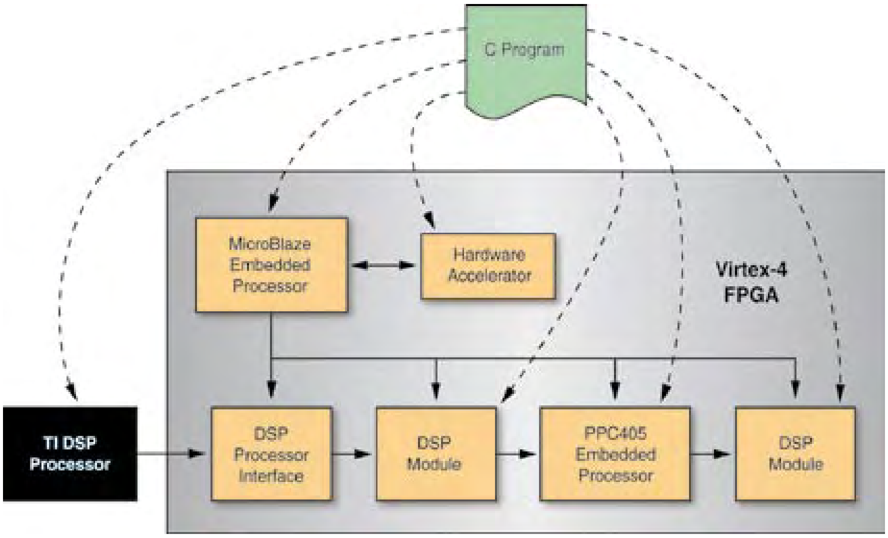

Figure 2

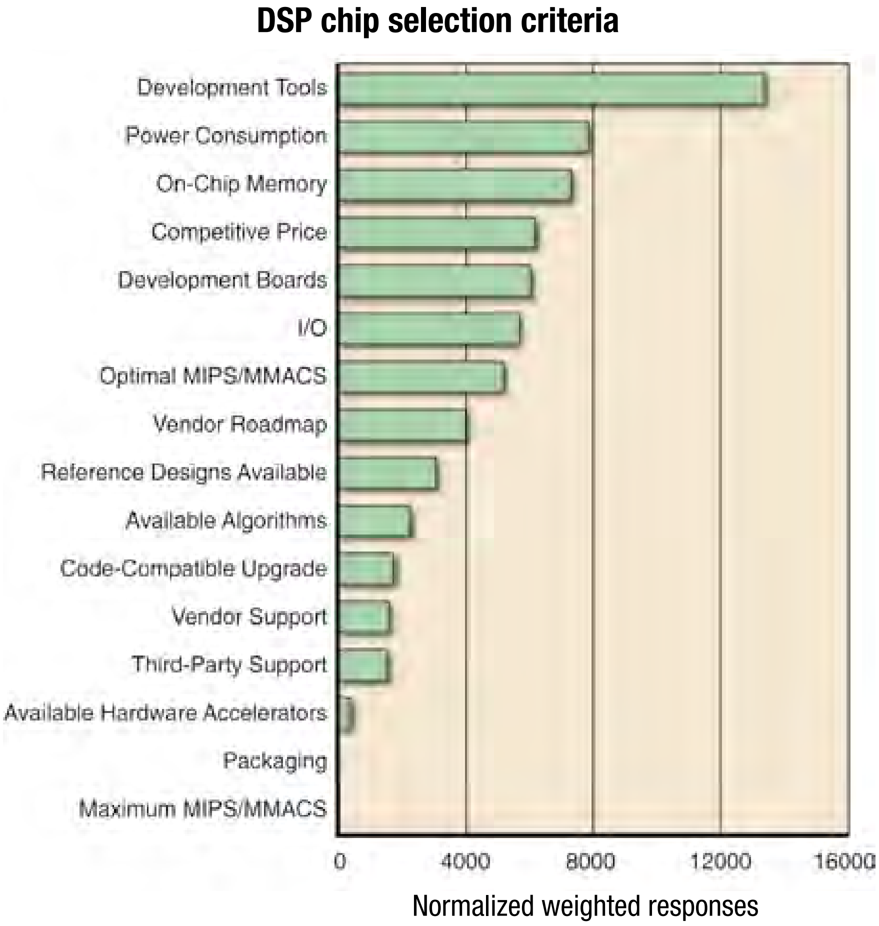

Figure 3

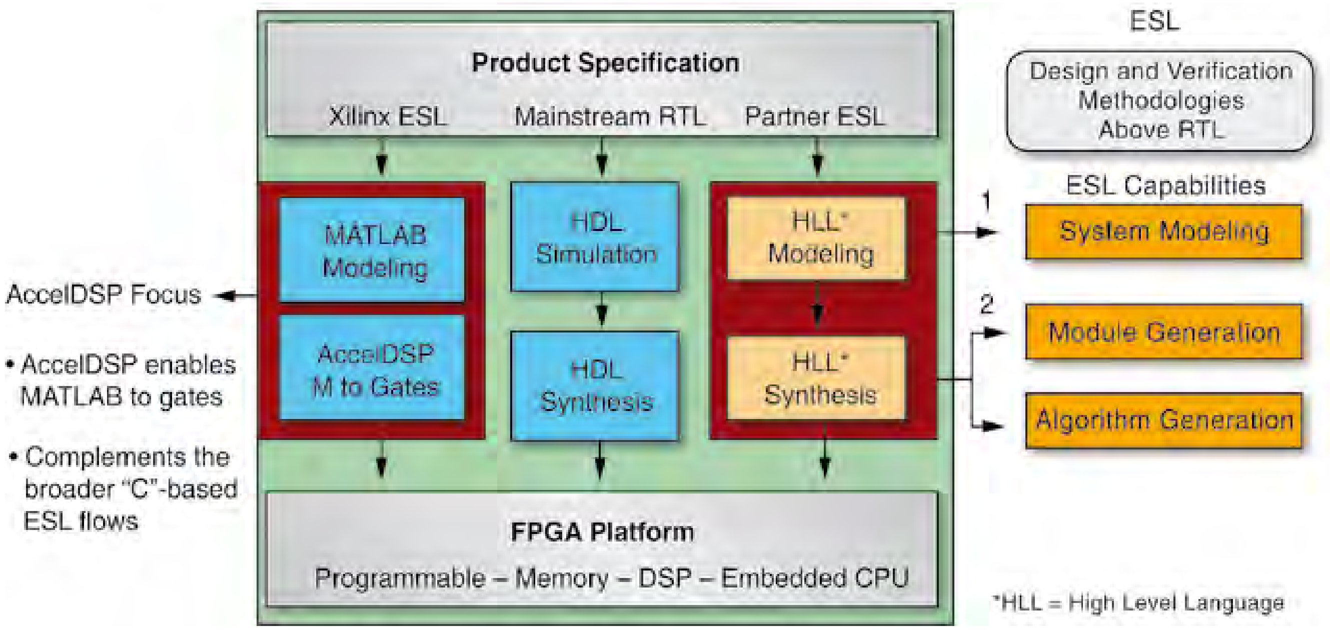

Figure 4

The performance requirements for mapping C routines into hardware accelerators are typically less aggressive. Here the objective is to accelerate the performance beyond that of pure software while maintaining a software-friendly design flow. Although the coding techniques and in-line synthesis instructions are still available, you can typically achieve your desired performance gains without their use.

Design methodology – the barrier to adoption

The effort and breadth of skill required to correctly partition and implement a complex DSP system is formidable. In 2005, the market research firm Forward Concepts conducted a survey to determine the most important FPGA selection criteria for DSP. The published results, shown in Figure 3, identify development tools as the most important. [Editor's note: Will Strauss from Forward Concepts writes the Forward Thinking column for DSP-FPGA.com.]

The survey illustrates that the benefits of a DSP hardware system utilizing an FPGA coprocessor are well understood, but that the current state of development tools represents a significant barrier to adoption for traditional DSP designers.

The Xilinx ESL Initiative

ESL design tools are pushing digital design abstraction beyond RTL. A subset of these tool vendors are specifically focused on mapping system models developed in C/C++ into DSP hardware systems that include FPGAs and DSP processors. Their vision is to make the hardware platform transparent to the software developer (see Figure 4).

Rather than attempting to solve one piece of this methodology puzzle internally, this year the company launched a partnership program with key providers of ESL tools called the *ESL Initiative*. The focus of this partnership is to empower designers with software programming skills to be able to easily implement their ideas in programmable hardware without having to learn traditional hardware design skills. This program is designed to accelerate the development and adoption of world-class design methodologies through innovation within the ESL community.

When combined, the collective offerings from Xilinx ESL partners offer a wide spectrum of complementary solutions that are optimized for a range of applications, platforms, and end users. Xilinx too has focused its efforts on complementary technology. For example, AccelDSP Synthesis provides a hardware path for algorithms developed in floating-point MATLAB, while System Generator for DSP allows modules developed using ESL designs to be easily combined with Xilinx IP and embedded processors. The quickest path to realizing a programmer-friendly FPGA design flow is through a motivated and innovative set of partners.

For more information about the ESL Initiative, visit www.xilinx.com/esl.

***Tom Hill** has more than fourteen years experience in the EDA industry. Hill oversees all product, strategic and corporate marketing activities related to the Xilinx development tool System Generator for DSP. Hill was most recently at AccelChip Inc., where he was technical marketing manager responsible for product direction and application of high-level design methodologies and tools for DSP applications. Prior to AccelChip he held positions as product manager, technical marketing manager, technical marketing engineer and field applications engineer for various FPGA and ASIC synthesis tools companies. Hill began his career as a hardware and ASIC design engineer at Allen-Bradley and Lockheed. Tom Hill holds a B.S. degree in electrical engineering from Cleveland State University.*

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Turning Software into Silicon

The processing challenges in making network-centric warfare a reality

By Neil Harold

With military applications demanding greater processing capability under tightening size, weight and power constraints, many developers are assessing the potential of alternative processing technologies to deliver the next step improvement in performance. Field Programmable Gate Arrays (FPGAs) and the Cell BE Processor are garnering a lot of interest, but there remain challenges to making full use of the potential of these technologies. What are the challenges to integrating these technologies into military embedded systems? And just how much performance benefit can developers expect when mapping real world applications to these architectures?

The world of processing technology is changing. Relying on Moore's law for performance improvements is no longer a guaranteed path to success, and device vendors are now considering a variety of approaches aimed at continuing the upward performance trend for next generation processing applications. This article looks at two of the highest profile technologies looking to obviate the limitations of traditional processing architectures – FPGAs and the Cell BE processor from IBM.

Nowhere is the demand for processing capability more acute than in military applications, where recent radical changes in the type of battle being fought have led to an emphasis on persistent surveillance, placing pressure on military technologies to deliver capabilities required for network-centric warfare. As doing "more with less" becomes an increasingly important strategy in military applications, developers are looking to alternative processing technologies to deliver the performance required within the size, weight, and power constraints of the wider system.

As two of the technologies garnering significant interest from military developers, FPGAs and the Cell Processor both offer a step improvement in performance capability compared with traditional processing architectures, but what are the challenges to these technologies really establishing themselves in the Defense market?

The importance of acceptance

In many ways, FPGAs can be considered the archetypal disruptive technology – highly powerful but difficult to master. Gradually however, they have achieved acceptance particularly among those who needed them most – developers of embedded military applications. This acceptance is due in no small part to the various advancements in FPGA technology in recent years, both at a device level and in the wider ecosystem. The advent of multi-million gate devices, embedded microprocessors, dedicated signal-processing units and high-speed serial links has made FPGAs increasingly competitive in both high and low-end embedded applications. Critically, these features have helped invoke a realization that FPGAs can perform floating point arithmetic – the latest Virtex-4 family from Xilinx offers a peak performance of 100GFLOPs.

Significantly for the Defense industry, there is now a wide selection of COTS vendors offering FPGA technologies on hardware platforms across a variety of forms and architectures, ranging from the FPGA-centric to the coprocessing approach. The last 2 years has also seen a marked change in the FPGA community with initiatives such as OpenFPGA (www.openfpga.org) demonstrating the type of collaborative approach that will deliver longevity to the COTS FPGA market and ultimately deliver the benefits of choice to the end users.

At a device level the Cell Processor, released by IBM in 2005, offers the type of processing performance that, much like FPGAs, makes for a compelling proposition. With a peak performance of 200GFLOPs it has huge potential for the type of real-time data intensive applications so common to the military. But achieving formal acceptance in the Defense world is a long-term play, as the FPGA community knows only too well.

With acceptance of the Cell processor in mind, the single biggest concern for military users is likely to be the fact that only one COTS vendor currently offers Cell-based platforms. This gives rise to sole source concerns, with many military programs looking for the reassurance of being able to procure similar products from other vendors. Acceptance also stems from a confidence in the longevity of a technology, which again puts a question mark against the Cell. As a new device, the Cell has no historical demonstration of technology updates while as a reference point Xilinx recently announced its 5th generation of the Virtex family of FPGAs. There is also uncertainty over the long-term future of the Cell. As the processing engine in Sony's flagship Playstation-3 gaming platform (see Figure 1), short-term volumes are virtually guaranteed. But the gaming industry is notoriously fickle and it's not clear at this stage whether the Cell will be updated for inclusion in the "Playstation-4" or whether another new technology will take its place.

Figure 1

SWAP

As mentioned at the outset of this article, military developers are under strict constraints when putting together embedded processing systems. Size and weight of both FPGA and Cell-based platforms will be a significant improvement on existing architectures, due to the reduction in overall quantity of processors required.

Power consumption has been a key factor in FPGAs gaining traction in military applications. Although the power rating of any device varies significantly depending on the application and clock speed it is running at, a range of 15-20W is a good estimate of the maximum power consumed by any member of the Virtex-4 family from Xilinx. Power consumption information for the Cell processor is hard to find, but estimates suggest that 70-80W can be expected. The difference between FPGAs and the Cell processor is mainly down to the 3.2 GHz clock frequency of the Cell, compared with the much lower 300-500 MHz rating of the FPGA.

Design challenges

No matter how compelling any processing technology is, for it to be successful it must provide a toolset and design flow that permits creation of complex applications.

Historically, this has been an area of significant challenge for FPGAs, where specialist skills and detailed architectural knowledge are deemed to be prerequisites for implementing high performance applications. The "blank" architecture of FPGAs is what simultaneously makes them hugely powerful and very difficult to program. Although there has been considerable progress in the development of high-level tools for FPGAs, with support for languages/tools such as C, MATLAB and Simulink, there remains a significant gap to be bridged before FPGAs can be programmed by users with no prior knowledge of the architecture. Work in this area would benefit considerably from greater collaboration amongst the tool and device vendors to build more cross-compatibility than is currently available, both at a card and device level.

The Cell processor is similar in the sense that the parallel architecture of the device can deliver huge performance benefits while presenting a sizeable programming challenge. The processing engine of the Cell is based on 8 Synergistic Processing Elements (SPEs), along with a Power Processor Element (PPE) for management purposes, all interconnected by a high-speed Element Interconnect Bus (EIB). Each SPE contains a Processing Unit (SPU) capable of integer and floating point arithmetic, along with a local 256 KB store and a 128x128-bit register set. From a programming perspective, the key aspect of this architecture is its complexity. Programming one of these SPUs is not an insignificant task, but mapping an application across all eight SPEs – which will be necessary to gain the type of performance available from the Cell – will require detailed planning and understanding of the target architecture both of which will add significantly to development timescales. Furthermore, the ecosystem that has started to emerge in the FPGA community will take time to form for the Cell processor and may well be stifled by the lack of a wider COTS support base (see Table 1).

> *"The ecosystem that has started to emerge in the FPGA community will take time to form for the Cell processor and may well be stifled by the lack of a wider COTS support base.*

Examples of Development Tools

Design Language	Tool	Vendor
HDLs	Active-HDL	Aldec
	Leonardo Spectrum	Mentor Graphics
	Synplify	Synplicity
	XST	Xilinx
C/C++	DIME-C	Nallatech
	Handel-C	Celoxica
	Impulse-C	
	Mitrion-C	Mitrionics
Simulink	System Generator	Xilinx
MATLAB	AccelDSP	Xilinx

Table 1

Device	Fab process	Peak Performance	Peak Clock Frequency	Max Logic Cells	Max Memory	LUT Type	Power Consumption
Virtex-5	65 nm	172 GFLOPs[1]	550 MHz	331,775	1.3 MB	6-input	35-40% power reduction in Virtex-5
Virtex-4	90 nm	110 GFLOPs[2]	500 MHz	200,448	1.24 MB	4-input	

Notes

1: Peak performance achieved using V5-LX330 and 400MHz clock frequency
2: Peak performance achieved using V4-LX200 and 350MHz clock frequency

Table 2

Portability and technology upgrades

Another factor that developers will have in mind when considering these technologies is how they plan for technology upgrades. Portability has been underestimated as a success factor in the microprocessor world, often taken for granted by developers looking to port existing applications onto the latest technology. Given that processing technology can evolve 5-10 times during the lifecycle of a standard military program, it is clear that military developers have a keen interest in being able to port from one release of a technology to the next.

FPGAs deliver a certain class of portability between different evolutions of device families and even between vendors. Moving from one version of a device family to the next – say Virtex-4 to Virtex-5 – is a very straightforward task (see Table 2). Clearly, where a design uses a piece of fixed silicon such as the embedded DSP Blocks in the Virtex family, to achieve comparable or better performance it is necessary that the next generation device has support for this feature. The silicon vendors have historically been very good at this type of backwards compatibility. Even porting from a Xilinx Virtex-4 device to a Stratix-II from Altera is a relatively simple task, with HDL acting as a kind of middleware that is agnostic of the hardware architecture being targeted.

The novel architecture of the Cell BE will make porting applications from traditional microprocessors a challenging proposition. Although the language may stay the same, the parallel architecture, as highlighted earlier, will demand reworked code in order to even get an application functioning correctly, never mind achieving an increase in performance. Portability is also hugely constrained by the fact that the Cell is a one-off device, with no equivalent alternative technology available from other vendors. Future portability is also an unknown quantity given that the long-term roadmap for the Cell is still unclear and potential users can't even derive comfort from having millions of devices across multiple generations deployed and in use.

Conclusion

As processing technologies continue to change, there is no doubt that the Cell processor and FPGAs will compete, particularly in military applications. The decision over which option to take will be influenced by a range of dynamics, but it could yet be that a rounded ecosystem will prove to be a decisive factor in convincing users to adopt a particular technology. On this basis, it appears that even the Cell with its mighty backers has some way to go before it establishes itself as a viable alternative to the current "alternative" processing technologies.

***Neil Harold** is experienced in development of embedded processing systems, with specialized experience in FPGA technology, including high-level design tools. Neil worked on the development of products and applications across a wide range of Xilinx FPGAs, from the original Virtex and Spartan families through to the latest Virtex-4 devices, and has skills in high-speed digital and analog hardware design. Neil has recently worked in a sales and marketing role, combining technology expertise and customer interactions to provide program management assistance and build awareness of market trends.*

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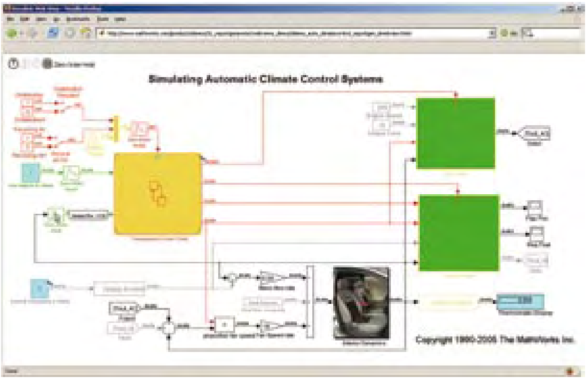
EDITOR'S CHOICE EDITOR'S CHOICE

Model-driven HDL code generator for FPGAs


Simulating Automatic Climate Control Systems
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Imagine generating *synthesizable* code from models, and you've conjured up The MathWorks' Simulink HDL Coder. Target-independent Verilog and VHDL code and test benches are created from models originating in the company's Simulink and Stateflow design suites. The game-changing software brings the promise of ESL system design that much closer to reality, for use in ASICs, ASSPs, and FPGAs. Going from high-end model straight to code that can actually be used in silicon saves time, cost, and errors – and is one step closer to design nirvana. [Editor's note: refer to Editor's Insight, page 7.]

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Facing component obsolescence

Phoenix or a Sitting Duck – what will be your response to RoHS?

By Lawrence Ricci

The European Community has adopted RoHS (Reduction of Hazardous Substance) guidelines that seem to be forcing many semiconductor components into premature end-of-life situations, often with no pin-compatible replacement. OEMs, dependent on these components for products with long life in the market, are in a quandary. Should they redesign, or make a 'lifetime buy' of the EOL components? In this article, Lawrence suggests the companies who adopt lifetime buy strategies will become 'Sitting Ducks' in the competitive arena, while more adaptable companies will emerge from the EOL RoHS fire as the 'Phoenix' with even more features and a stronger customer value proposition. The best solution to RoHS/EOL may be to adopt fast turn design methodologies and accelerate the development of more competitive products.

A few years ago when the RoHS initative was being developed, it seemed it would have a soft impact on high-tech OEM devices. This has proved not to be true. The tiny amount of lead-based solder on PCBs is of issue, and the even smaller, microscopic, quantity of lead inside semiconductor chips is of issue as well. Semiconductor suppliers, always ready to move to next-generation technology, were quick to issue end of life (EOL) notices for non-RoHS parts. Pin-compatible, RoHS compliant parts are often not available. This earlier than-expected component obsolescence, from the semiconductor side, impacts all OEMs, including OEMs like medical device manufacturers who were supposed to be shielded from direct application of the RoHS statute. These OEMs are now seeking alternatives.

Figure 1 compares web searches and job advertising for the term RoHS (Blue) and, just for comparison, ISO9001 (Red/Orange). These trends demonstrate an interesting societal comparison. Notice that web searches (on Google) for RoHS have been rising steadily for two years, mostly from Asian locations. Presumably, those engineers are now trained and ready. As evidence of this, the "flags" A to E denote press releases mentioning RoHS compatible products.

Figure 2 (courtesy Indeed.com) is placed below congruent time periods Figure 1 and shows US job advertising containing the terms RoHS and ISO9001. Notice how much later the US companies developed an interest in the RoHS issue, and when they respond they search for people, not information. The EU compliance date is only four months past this chart, so it is probably 'too late' for those new jobs to have much of an impact. In short, RoHS is affecting companies worldwide.

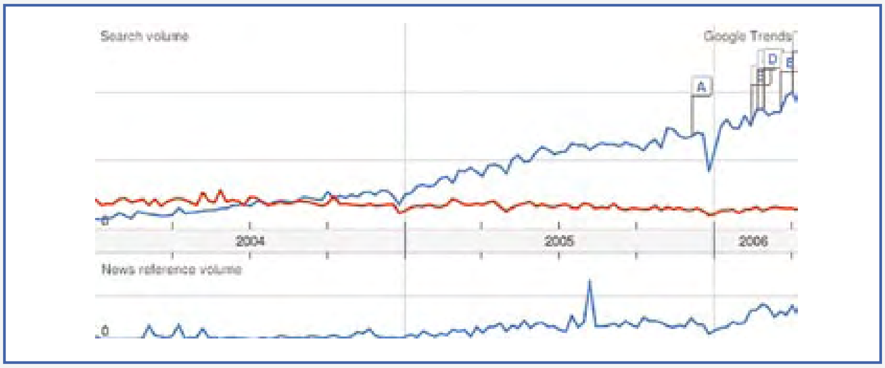


Figure 1

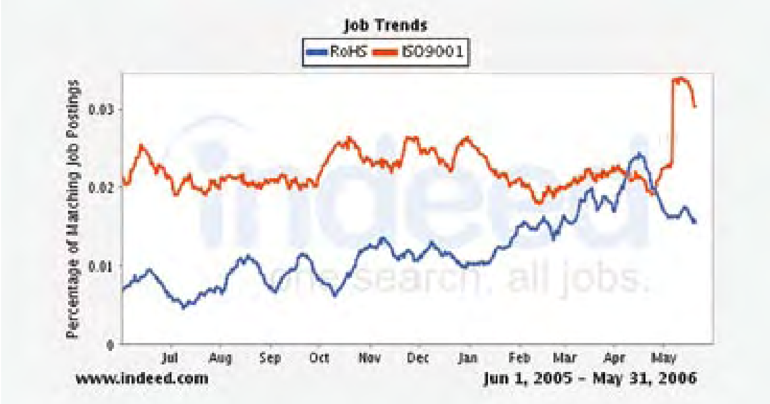


Figure 2

Lifetime buy or redesign – be a Sitting Duck or a Phoenix?

The tradeoff is simple - make a lifetime buy of the non RoHS chips and fight approvals on a case by case basis, or design a new product with compliant parts and enhanced features. The two approaches differ in cost, risk and potential benefit. Ultimately, the measurements of cost, risk and benefit are made in a competitive area, where the wisdom of each OEM's choice is compared, by the invisible hand of the market, to the choices of the OEM's competitors. The real impact of the choice the OEMs make today may not be known for years, or even a decade, but it is likely to have a dramatic and definitive impact, well understood in retrospect.

The powerful dynamics associated with RoHS impact became evident when two OEMs contacted Applied Data Systems in the same week. For several years, these companies (in completely different industries) have been evaluating the move to a next generation product, but have not yet made the commitment for a new design. Suddenly, the same week, both companies moved their programs to the front burner. Why? Because both companies got the same EOL notice and needed to either buy a million dollars' worth of inventory, or accelerate a redesign/replacement program. They were faced with the *Sitting Duck* or *Phoenix* choice.

> *The RoHS-linked EOL notices, however, injected a laser clear demarcation into their planning. A line was drawn in the sands of time.*

Both companies are major enterprises, and both have been wrestling with powerful but sometimes ill-defined constraints and objectives from their markets, their technologies and their internal politics. The RoHS-linked EOL notices, however, injected a laser clear demarcation into their planning. A line was drawn in the sands of time. Both companies had to decide what to do, and had to put a million dollar investment into either (a) obsolete inventory or (b) a new product design. Failure to pick one path or the other would be tantamount to withdrawal from their business segment. While there are creditable, defendable Phoenix and Sitting Duck options, the *dead duck* option is not really a business proposition management can take to shareholders. These companies, and countless others, are making the Sitting Duck or Phoenix tradeoff now.

Tradeoff: Cost

The initial lifetime buy is just the first of many costs the Sitting Duck must pay. During the period of EOL, other components will disappear from the supply chain, in fact at an increasing rate. Many of these will have no pin-compatible replacement, so more lifetime buys will be required.

From a business point of view, inventory is NOT *money in the bank.* In business, *money in the bank* pays interest. *Aging* inventory does the opposite – the company must reserve income each quarter against eventual write off. In other words, a company buys inventory with cash, and then, in turn, gets a constant drain on its income. Depending on the GAPP standards invoked, a million dollars of inventory could demand tens of thousands of dollars per quarter from income (e.g. *margin*) just to ballast down the ballooning balance sheet of its Sitting Duck.

Commitment to a *lifetime buy* is a costly strategy. The initial cash demand is typically more than the all-in product development cost, and the implied commitment to subsequent lifetime buys multiplies the eventual cost.

Tradeoff: Features

The EOL buy does allow the continued supply of the 'same old product'. The problem is today's dynamic and international markets demand feature enhancement. Devices that were once stand-alone single purpose devices built on 8-bit micro technology are now part of powerful systems. Users want network interfaces, web accessibility, graphics, and other high-end functions that they get and expect, in devices as modest as cell phones and thermostats. Likewise, as the users have seen functions go up, costs have come down.

Even so, there are markets where features remain static for decades, like certain power meters used in electrical utilities. Each OEM who evaluates the Sitting Duck strategy must ask himself – does he work in a market where his existing feature set and price point can remain static for the duration of his lifetime buy?

Tradeoff: Risk

OEMs always want a new product, but the risk development can halt action. Many projects, once started, never finish. When the continued supply of the older product is not assured, the risk is serious. Risk is why both the companies that began the ADS investigation into RoHS EOL did not start their programs years ago. But now, paradoxically, risk avoidance may compel them to move forward.

If there are multiple competitors in a business sector, some will choose the *lifetime buy* Sitting Duck option and some will choose the *accelerated design* Phoenix option. These opening moves may set the pattern of competition for a decade or more. The companies who select the stasis of a lifetime buy strategy will become the Sitting Duck targets with fixed features and cost. Eventually, one of the companies that adopts the more flexible Phoenix fast turn development options will get the duck in its sights and pick it off.

There are unseen competitive threats as well. The OEM needs to realize that his pond is open to the sky – new birds can fly in from super-competitive Asian factories at any time. A few fat and happy Sitting Ducks are how these more competitive birds can best find, and eventually own, the pond.

In fact, the situation for the Sitting Duck is even riskier; it goes beyond competitive forces. Other non-competitive forces like additional regulation or broad industry shifts could intervene during the period of their 'lifetime buy' and render the product, and its millions of dollars of inventory, valueless.

Minimizing risk for fast turn development

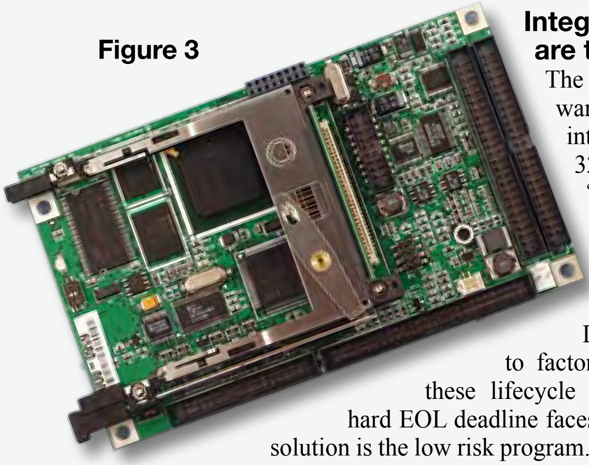
So, faced with a supply side EOL decision, the path forward is best understood as a risk vs. risk decision. The risk of a Sitting Duck strategy, while not immediate, is there to estimate and live with. The risk for fast-turn development, however, can be reduced.

The risk of moving to a feature-rich 32-bit embedded system is real, and frequently underestimated by the OEM who has prior experience with simpler 8- and 16-bit systems. Methodologies of development must change; the learning curve to work in the 32-bit world can be steep. But in short, the best risk-avoidance strategy is to buy in what you can, and design and build what you must.

The IP the OEM's customers value most is usually based on the OEM's sensors and application software. This is the core technology he must protect and develop. No matter how complex, elaborate and difficult to develop, platform technology including networking, graphics, security and so forth are commodities designed against industry standard compatibility specs. Vintners make wine, they don't make the bottles. OEMs, especially OEMs pressured by EOL choices, should focus on their core value.

By outsourcing platform components of their system, the OEM can begin application development on day one of the project, dramatically reducing risk. Indeed, it may be possible to have a proof of concept OEM device running in a few weeks or months, before the final choices must be made about EOL lifetime buys. Then, moving past proof of concept, the OEM needs to find the low-risk path forward to volume production.

Figure 3



Integrated platform solutions are the low risk alternative

The use of a RoHS complaint hardware solution like an ADS BitsyXb, integrated by the supplier with a 32-bit OS may not yield the lowest 'hardware' cost, but often yields the lowest product lifecycle cost (Figure 3). Lifecycle cost is more than development cost and production cost – it spans the full DIME of Development, Introduction to factory, Maintenance and EOL. All of these lifecycle costs are important, but when a hard EOL deadline faces the OEM, the integrated platform solution is the low risk program. All hardware and software is there, tested and in fact proven in dozens of applications. A custom build of the OS can be done in a few days, presenting the OEM with exactly his target application environment. And once critical deadlines are met, and there are paths for cost reduction.

ADS can move from standard product like the BitsyXb, designed to mate with the OEM's mother board, to low cost single-board designs incorporating the OEM's circuit design and made just for the OEM under an exclusive supply agreement. At higher volumes, even the production of this board can be transferred to the OEM's factory or designated CM. And, of course, once the Phoenix OEM has completed his first post EOL rebirth, he can potentially do his own design, with or without ADS, for the subsequent generations.

Conclusion

We live in dynamic times; change is forced at us from all directions. In the evaluation of *purchased platform* vs. *internally engineered* products, there is always a tradeoff between margin and speed of development. In this case, where entire industries are faced with simultaneous EOL notices, this choice may be the choice to be a Sitting Duck or a phoenix.

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TMS320F240x			Yes	Yes	Yes	Yes	Yes	
TMS320F28xx			Yes	Yes	Yes	Yes	Yes	Yes
TMS320C54x™			Yes	Yes	Yes	Yes	Yes	Yes
TMS320C55x™			Yes	Yes	Yes	Yes	Yes	Yes
TMS320C6xxx™			Yes	Yes	Yes	Yes	Yes	Yes
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TMS470 ARM7			Yes	Yes	Yes	Yes	Yes	Yes
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RoHS:
Yes, it affects *you*

By David Compston

There are three common misperceptions about the RoHS (restriction of the use of certain hazardous substances) legislation that came into force within the European Union on July 1, 2006. The first misconception is that it only affects Europeans. The second is that it only affects manufacturers and suppliers in the commercial – rather than the military – marketplace. The third is that the primary issue at stake is the problem caused by tin whiskers. The author will show how RoHS legislation affects the United States as much as it affects Europe; how the commercial reality of COTS computing means that, while defense electronics are nominally exempt, they will actually be forced to become RoHS-compliant; and how, while tin whiskers may have received the most attention, the real problem of lead-free manufacturing lies in the need to develop a repeatable process that can guarantee 100 percent reliable joints using lead-free solder.

The RoHS directive is a European Union (EU) directive and is part of a broader effort (including directives such as *WEEE*, which deals with the collection, treatment, recycling, and disposal of waste electrical and electronic equipment) that is designed to minimize electrical products' impact on the environment. RoHS deals with "the restriction of the use of certain hazardous substances in electrical and electronic equipment," and bans the placing on the EU market of new electrical and electronic equipment containing more than agreed levels of lead, cadmium, mercury, hexavalent chromium, Polybrominated Biphenyl (PBB), and Polybrominated Diphenyl Ether (PBDE) flame retardants as of July 1, 2006. It is, however, the subject of several misconceptions.

Misconception 1: Only a problem in Europe?

While much attention is focused on the RoHS directive, it should be noted that Europe is not alone in pursuing policies designed to minimize the harm done to the environment by certain metals. Japan, for example, is one of the world's foremost producers of electronic components and printed circuit boards. In 1998, when the Japanese government increased levies for recycling equipment that used lead in its manufacture, Japanese industry began an aggressive program to remove lead from the manufacturing process (probably the single largest impact of the RoHS directive is on the use of lead, particularly in solder).

RoHS misconceptions

1. It only affects Europeans
2. It affects commercial, not military, suppliers
3. The primary issue is tin whisters

In the United States, the state of California has also begun to respond to increasing consumer demand for environmentally friendly products and processes. In September 2003, the state enacted legislation that funds electronics recycling programs by adding a tax on the sale of televisions, monitors, and flat panel displays. The California legislation also contains "RoHS equivalency" measures that prohibit the sale of any electronic product in the state that would be prohibited from sale in the European Union because of the presence of heavy metals. The deadline for compliance with this legislation is January 2007. It therefore becomes true that it is no longer the case that the European Union market requires RoHS compliance, while the U.S. market does not; the U.S. market is becoming divided between states requiring it – California was the first, but others are expected to follow – and those that do not.

And while the adoption of *green* manufacturing policies in Asia has typically lagged behind the rest of the world, many Asian electronics manufacturers in countries such as Korea, Taiwan, and Malaysia are discovering that the major customers on whom their businesses depend will only do business with suppliers capable of delivering RoHS-compliant components and subsystems. Even China – considered by many to be a laggard in environmental issues – is in the process of enacting legislation similar to RoHS, but even more stringent.

The European Union legislation, therefore, is reflective of a worldwide trend. In theory, RoHS is indeed a Europe-only issue, insofar as it prevents placing on the European Union market any product that is not RoHS-compliant, wherever it is manufactured, unless that product is exempted from compliance. However, the European market for electrical goods comprises a significant proportion of the total worldwide market: The population of the European Union countries is 377 million versus the 289 million population of the United States. Also, the majority of today's electrical and electronic products are produced by global manufacturers for a global market. Therefore, as with manufacturers' decisions as to whether they will support both commercial and military versions of the same product, manufacturers must also decide whether to support European and non-European versions of the same product. Most manufacturers are preferring to harmonize and standardize manufacturing policies and processes on a worldwide basis – implying support of only a single, worldwide (and thus RoHS-compliant) version of a product. This is likely to mean that the majority of electronics products sold in North America will be RoHS-compliant.

This is no less true for military, aerospace, and defense suppliers who anticipate a worldwide market for their products and solutions. If it is their intention to make a platform, a subsystem, or a weapon available on a global scale, it will make little sense to design and engineer one non-compliant version for the home market and another RoHS-compliant version for the overseas market.

Misconception 2: Not a problem for military applications?

But aren't electronics for defense applications exempt from RoHS compliance? The answer is, "Yes, in theory." However, the commercial reality is likely to dictate otherwise. Products designed specifically for military, aerospace, and medical applications are mostly exempt from the RoHS directive. The reality, though, is that the military market now relies heavily on Commercial Off-the-Shelf (COTS) solutions. The advantages of COTS solutions are lower acquisition costs, lower lifetime ownership costs, and increased technology insertion opportunities.

Thus, because the components used in military computing are also, by definition, widely used in nonmilitary applications and because it makes little financial sense for component manufacturers to support two parallel product lines – one RoHS-compliant for commercial applications, and one that is not RoHS-compliant for military applications – component manufacturers are migrating toward the support of only RoHS-compliant products. Therefore, the majority of devices used by the military will, by definition, be RoHS-compliant.

Some manufacturers have announced an intention to continue to manufacture non-RoHS-compliant parts. However, because these will not be parts made for the broad commercial market, they will no longer be COTS parts. Thus the COTS advantages will be lost, notably: Decreased demand and smaller production runs will likely see costs escalate while continuing availability of a *minority interest* part will be far from assured, increase lifetime ownership costs, and substantially narrow technology insertion opportunities.

So, like it or not, RoHS is a reality for military organizations worldwide. But why is there so much concern about it? The fact is that lead has been a key material in the manufacture of electronics components and subsystems for a long time. It is a known and reliable ingredient, and eliminating it from well-established manufacturing processes means either finding an equally reliable alternative or re-engineering those processes.

Misconception 3: It's all about tin whiskers, then?

The challenge that has received the most attention in any discussion about the impact of RoHS has been the phenomenon known as *tin whiskers*. The tin whisker is not a new phenomenon nor is it specific to RoHS. It was first identified in electroplated cadmium components during the late 1940s. It is widely believed that lead, when alloyed with tin and forming as little as 2-3 percent of the solder, imparts whisker-inhibiting attributes to the solder. The RoHS focus on the elimination of lead has in turn focused attention on tin whiskers.

While it is possible to have gold, silver, and zinc whiskers, tin is the most prone to the crystalline metallurgical phenomenon in which the metal grows tiny *hairs* or electroconductive filaments that emerge at right angles to the underlying metal. (See Figure 1, courtesy of I. Hernefjord and NASA Goddard). The whiskers can grow as long as 10 mm but are more typically less than 1 mm in length. It's an effect that's mostly seen on elemental metals but that can also occur with alloys. Why whiskers grow is not yet well understood. The presence of compressive mechanical stresses including those induced by electroplating, mechanical stresses (torquing a nut or screw), thermally induced stresses, and stresses induced by the diffusion of different metals appear to encourage tin whisker growth.

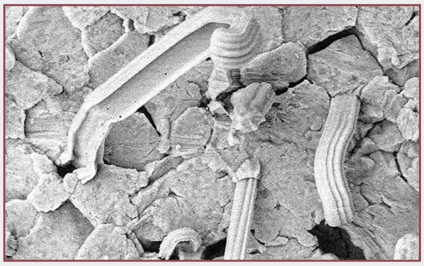

Figure 1

Tin whiskers can carry a current of up to 10 mA, which means that shorts caused in high-voltage, high-current circuits will quickly burn out; in low-power circuits, they will tend to cause intermittent failures. They also have an incubation period that can be up to several years: as such, a component that appears whisker-free can, in fact, develop whiskers much later. This is less of an issue for commercial/consumer products with their expected short lifetimes, but for extended-service-life military and avionics platforms such as satellites, aircraft, helicopters, and even missiles in storage, it can be highly problematic; whereas the formation of tin whiskers is unlikely to cause more than temporary and inexpensive inconvenience to consumers, the implications for mission-critical applications and platforms can be substantially more serious.

Radstone's position is that the tin whisker phenomenon is only applicable to fine pitch (0.001 inch) components that have a 100 percent electroplated tin leg finish, regardless of the type of solder used. The company's policy is to:

- Avoid the use of fine-pitch components with electroplated tin leg finishes
- Select devices that have a tin alloy comprising at least 2 percent bismuth or similar
- Reflow the legs to alleviate the stress that causes tin whiskers

In the long term, it seems likely that the component industry will move to tin alloys.

The really significant issue

For the military, however, it is vital to focus on a potentially much more significant issue: the issue of the reliability of joints made with RoHS-compliant, lead-free solder. For example, the lead-free replacements for conventional Sn60/Pb40 (60 percent tin, 40 percent lead) solder have higher melting points, requiring re-engineering of many of the components and materials used in electronic assemblies. Typically, lead-free solders have a melting point of 260 °C, rather than the more *normal* 215 °C.

Lead-free solder joints may produce mechanically weaker joints depending on service and manufacture conditions, which may lead to a decrease in reliability in using such solders. This is a significant issue, and one to which Radstone has applied extensive expertise. Lead imparts a high degree of *elasticity* to solder such that, when a board is subject to temperature extremes – as is the case in many military applications – the solder can expand and contract without breaking. Removing lead from the solder means that the solder loses this flexibility and temperature extremes can cause it to crack, resulting in a failed joint. As with tin whiskers, this is not a problem for consumer products, which are seldom, if ever, subjected to harsh environmental stresses.

In the military world, however, lead-free plastic Ball Grid Arrays (BGAs) will require a lead-free solder and a fully lead-free build. After many months of effort, our company has now developed a proprietary process that has seen lead-free assemblies exceed more than 1,000 thermal cycles; first attempts had managed only two or three thermal cycles before failing. This represents a significant step forward in enabling the production of lead-free products that will meet the exacting reliability requirements of military customers.

There will unquestionably be a transition period during which customers will continue to demand, and will be able to acquire, products that are non-RoHS-compliant. Manufacturers will respond to this demand as long as it is feasible and practicable to do so, while developing parallel products that comply with the legislation for those customers requiring them. Inevitably, new products that come to market will be RoHS-compliant. The trick will be to maintain appropriate configuration controls as described by the Government Electronics and Information Technology Association (GEIA) document drawn up in association with the Aerospace Industries Association (AIA) and the Avionics Maintenance Conference (AMC) GEIA-HB-005-1, which describes the process for managing the transition to lead-free.

The future of military embedded computing and RoHS

Since July 1, 2006, RoHS legislation has affected military customers worldwide. The good news is that much of the work necessary has already been done by the leading companies in military embedded computing that will ensure that lead-free products for the military and defense market are no less reliable, no less robust, and no less dependable than their predecessors.

David Compston *is director of marketing at Radstone Embedded Computing. He began his career as a software engineer working in the UNIX arena with Plessey Microsystems. Following the management buyout of Plessey Microsystems to form Radstone Technology, David moved into marketing at Radstone Embedded Computing, a role in which he has responsibility for the strategic development of Radstone's embedded computing business. He earned his BSc in Computer Science from Warwick University.*

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Advertiser	Category	Page
Alpha Data	FPGA	75
Annapolis Micro Systems	FPGA	67
Annapolis Micro Systems	FPGA	68
Annapolis Micro Systems	FPGA	69
Annapolis Micro Systems	FPGA	72
Annapolis Micro Systems	FPGA	73
Annapolis Micro Systems	FPGA	76
Annapolis Micro Systems	Hardware	81
Annapolis Micro Systems	Hardware	85
BittWare	DSP Based Carrier Boards	53
Celoxica	FPGA	75
Celoxica	FPGA	77
ChipX	Hardware	86
Danville Signal Processing	DSP Resource Boards	59
First Silicon Solutions	Software	46
Gedae	Software	48
Hunt Engineering	DSP Resource Boards	58
Improv Systems	DSP Chips and Cores	54
Innovative Integration	DSP Resource Boards	55
Innovative Integration	DSP Resource Boards	58
Innovative Integration	FPGA	70
Innovative Integration	FPGA	71
Innovative Integration	FPGA	74
Innovative Integration	Software	52
Integrated Device Technology	Hardware	80
Kane Computing	Software	48
Lattice Semiconductor	FPGA	62
Lyrtech	FPGA	77

Advertiser	Category	Page
Nallatech	FPGA	63
Nallatech	FPGA	64
Nallatech	FPGA	65
Nallatech	FPGA	66
Nallatech	FPGA	59
Nallatech	Software	51
Radstone	DSP Based Carrier Boards	52
Radstone	FPGA	66
Radstone	FPGA	71
Radstone	Hardware	83
Radstone	Hardware	86
SPIRIT DSP	Software	49
Synplicity	FPGA	60
Synplicity	FPGA	78
Synplicity	FPGA	79
Synplicity	Software	50
Synplicity	Software Defined Radio	44
Synplicity	Software Defined Radio	45
Traquair Data Systems	DSP Resource Boards	56
Traquair Data Systems	DSP Resource Boards	57
Traquair Data Systems	Hardware	82
Traquair Data Systems	Hardware	84
Tundra Semiconductor	DSP Chips and Cores	55
VMETRO	FPGA	74
VMETRO	Hardware	83
Xilinx	FPGA	61
Xilinx	Software	47

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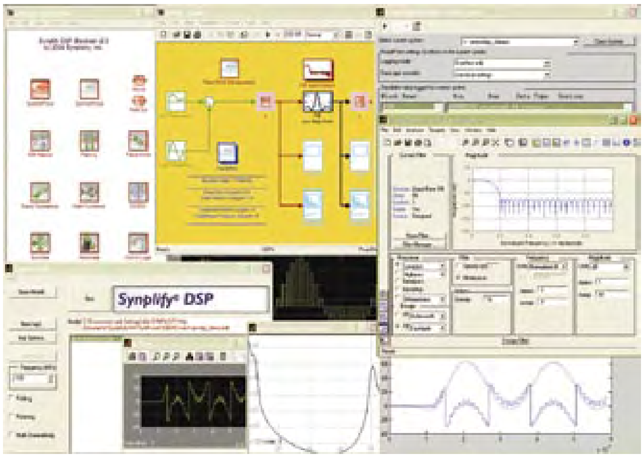

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www.synplicity.com

Simply Better Results

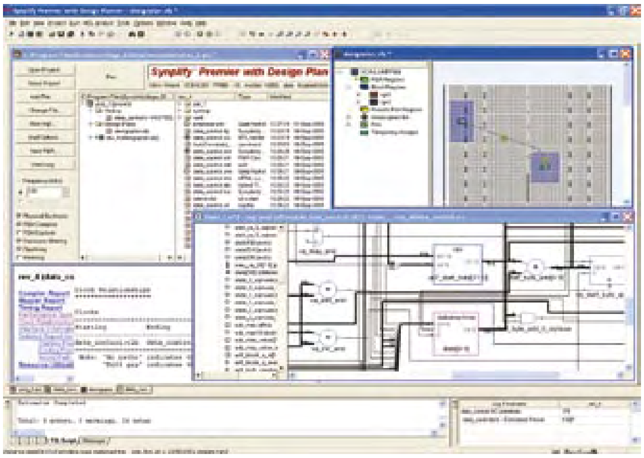
Synplify Premier

Synplicity's Synplify Premier software is the ultimate FPGA synthesis and debug solution. It builds upon Synplicity's industry-leading synthesis technology, and adds new graph-based physical synthesis for timing closure and simulator-like visibility into operating FPGA devices for fast source-level debug.

Graph-based physical synthesis – Synplicity invented graph-based physical synthesis to improve timing closure by means of a single-pass physical synthesis flow for 90 nm FPGAs. In FPGAs, unlike ASICs, proximity of placed logic does not imply better timing. The essence of the graph-based approach is that pre-existing wires, switches, and placement sites used for routing an FPGA can be represented as a detailed routing resource graph. The notion of distance then changes to a measure of delay and availability of wires. The Synplify Premier tool's graph-based physical synthesis technology merges optimization, placement, and routing to generate a fully placed and physically optimized netlist, providing rapid timing closure and a 5 percent to 20 percent timing improvement.

Best quality of results – The Synplify Premier product is a true timing-driven synthesis product, which means it delivers the timing performance you need in your design by automatically moving registers within combinatorial logic in order to balance timing delay and improve circuit performance up to an additional 20 percent Quality of Results (QoR).

Simulator-like visibility into a live FPGA – The Synplify Premier software provides a rapid method of finding functional errors in FPGA designs by providing simulator-like visibility into operating FPGA hardware. Synplicity's integrated debugging software, based upon technology from the Identify product, allows designers to annotate signals and conditions they want to monitor directly in their RTL code.



FEATURES:

- Graph-based physical synthesis – fast timing closure and a push-button performance boost of up to 20 percent
- True timing-driven synthesis – after meeting timing constraints, automatically optimizes your design for area/cost
- Automatic handling of DSP functions – infers DSP functions from RTL and maps into vendor's DSP hardware (i.e. MACs)
- Lightning-fast compile times – synthesizes even the largest design in a fraction of the time of other tools
- HDL analyst RTL analysis and debugging tool – instantly generates RTL block diagrams from your RTL code; helps identify critical paths
- Interactive timing analysis – enables point-to-point timing analysis without re-synthesis
- Automatic RAM inferencing – bypass tedious hand instantiation of RAM and makes your design technology independent
- FSM explorer – automatically finds and selects the best FSM coding style for the meeting your timing and area constraints
- Automatic retiming – moves registers automatically within combinatorial logic to balance delay and improve performance
- Integrated RTL instrumentation and debug – instrument and debug your design directly in your RTL source code
- Probe point creation – allows any signal to be tied to an external pin for testing without HDL code changes

For more information, contact: info@synplicity.com

RSC# 31749 @ www.dsp-fpga.com/rsc

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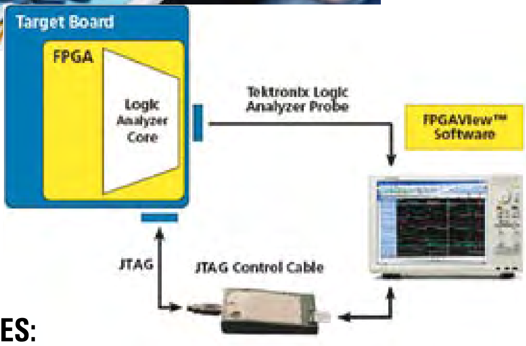
www.fs2.com

FPGAView Software for Tektronix Logic Analyzers for Debugging Altera and Xilinx FPGAs

The FPGAView™ software is a PC Windows-based program designed for use with Tektronix Logic Analyzers (TLA). It enables real-time debugging of Altera and Xilinx FPGAs. Using FPGAView, design engineers can quickly and easily measure signals inside their FPGA design and select which group of internal signals to probe without having to recompile their design. FPGAView simplifies logic analyzer use by automatically updating channel names with the internal signal names selected and providing a mechanism to auto-select channel groupings from the same selection.

FPGAView software makes debugging your FPGA design faster than ever, because the once tedious process of defining and routing the FPGA signals to the external logic analyzer connector and mapping channels for the logic analyzer are all handled by the FPGAView software. To learn more about the Tektronix Logic Analyzer (TLA), visit the web site at www.tektronix.com

The FPGAView software package works with a Tektronix TLA 5000 or 7000 series with Tektronix logic analyzer software version 4.3 or later. It requires the appropriate programming cable for the Altera or Xilinx FPGA, or an FS2 System Navigator probe. It also requires the use of the programming software from the FPGA vendor.



FEATURES:

- Speeds debugging of Altera and Xilinx FPGA devices with the Tektronix Logic Analyzer (TLA)
- Convenient control of the FPGA Logic Analyzer Interface (LAI) logic block Bank selection
- Identify and map LAI output pins to external logic analyzer connector faster than ever
- Automatic update of Tek Logic Analyzer (TLA) channel names when selecting a different signal bankWorks with Altera USB Blaster, ByteBlaster, or FS2 System Navigator probes or with the Xilinx programming cable
- Handles multiple LAI instantiations in one device for multiple clock domain support
- PC Windows user interface
- Supports multiple FPGA devices through JTAG chaining
- User can assign a TLA setup file for each bank, making it easy and automatic to reconfigure channel groupings

For more information, contact: info@fs2.com **RSC# 31713 @ www.dsp-fpga.com/rsc**

Xilinx

2100 Logic Drive • San Jose, CA 95124
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www.xilinx.com/dsp

XtremeDSP Development Tools

The XtremeDSP solution from Xilinx features the industry's most comprehensive suite of development tools to help you finish faster. The solution comprises algorithms, design tools, multiple development platforms, and award-winning technical support.

Xilinx System Generator for DSP (System Generator) is the industry's preferred tool for developing DSP onto FPGAs. The tool enables you to model, design, simulate, verify, and debug your FPGA-based DSP system, even if you don't write a word of VHDL or Verilog.

Model and design: Your system may contain FPGAs and DSPs in the signal chain. Model the entire system using Simulink and blocksets from the The MathWorks. Design the FPGA section using the bit and cycle accurate Xilinx blockset.

Import MATLAB algorithms: For complex MATLAB functions like linear algebra or matrix multiplies, import synthesized RTL code from the Xilinx AccelDSP™ tool.

Simulation and automatic HDL generation: Simulate your design in Simulink. You can also import legacy HDL code via a black box and simulate it in the loop using ModelSim®. When done, System Generator will automatically generate efficient HDL, or a netlist or a bit-stream at the push of a button.

Verification and debug: Verify your system on your target hardware using our high-bandwidth hardware-in-the-loop capability. Debug probes can be used to monitor the FPGA's internal nodes to reduce debug time.

XtremeDSP algorithms

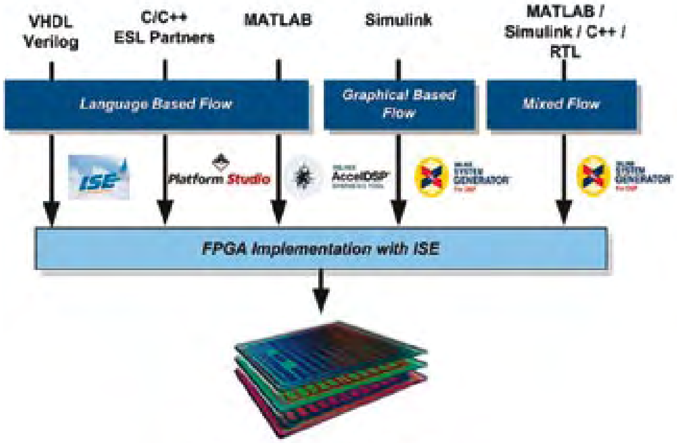
There are more than 60 DSP algorithms available from Xilinx and partners. Examples include Viterbi decoders, RACH designs for 3G systems, filters, FFTs, etc.

XtremeDSP development platforms

Choose from one of multiple XtremeDSP development platforms for standalone or DSP co-processing designs from Xilinx or partners such as Lyrtech, Nallatech or Sundance, or other Global Alliance member's.

Award-winning technical support

Count on our technical staff when you need it most to finish faster.



Supported DSP Design flows

FEATURES:

- Model and design your system using MATLAB, Simulink, and blocksets from The MathWorks
- Use the Xilinx bit and cycle accurate library for designing algorithms for the FPGA
- Import MATLAB algorithms like linear algebra and matrix inversion and multiplication
- Automatically generate HDL or a bitstream at the push of a button with no loss in performance over designs written in HDL
- Verify your system using hardware-in-the-loop; use chip-scope probes to speed up debug
- Choose from more than 60 XtremeDSP algorithms delivered as IP cores
- Choose from multiple XtremeDSP development platforms for video, digital communications or military applications like JTRS SDR
- Use our field DSP specialists or award-winning technical support
- Learn about our Virtex™-5, Virtex-4 and Spartan™-3/3E FPGAs for DSP; see the FPGA section
- Xilinx XtremeDSP education classes to help you finish faster

For more information, contact: narinder.lall@xilinx.com **RSC# 31771 @ www.dsp-fpga.com/rsc**

Gedae, Inc.

1247 N Church Street, Suite 5 • Moorestown, NJ 08057
Tel: 856-231-4458 • Fax: 856-231-1403
www.gedae.com

Gedae MDD for DSPs

Gedae is an integrated design environment for Model-Driven Development (MDD) of complex sensor processing applications based on DSP boards or distributed networks.

Gedae streamlines and simplifies the porting of applications to multiple DSP and FPGA processors. Its block diagram programming language specifies only the functionality of the graph, without regard to the target system. Gedae uses its knowledge of the target (processor layout, transfer methods, and optimized routines) to compile the block diagram into an efficient implementation of the application on the target processors. Detailed timing and visualization displays create an extensive debugging and analysis capability.

FEATURES:

- Supports all sensor based applications: RADAR, SONAR, LADAR, image, audio and communications processing
- Successful, deployed programs credit Gedae with helping them stay on time and significantly reduce costs
- Entire product life cycle, from research through embedded deployment, is done with one tool
- Creates and launches target executables for each processor with one button press
- Powerful analysis tools rapidly pinpoint problem areas and enable users to fix and rerun in minutes
- Dramatically reduces integration issues in sensor processing applications while also improving efficiency

For more information, contact: sales@gedae.com

RSC# 31714 @ www.dsp-fpga.com/rsc

Kane Computing Ltd

7 Theatre Court, London Road • Northwich, CW9 5HB GB
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www.kanecomputing.co.uk

Predator2 Emulator

The Predator-II combines the performance of a PCI emulator with the convenience of portable external emulators. The emulator uses the standard Texas Instruments unified drivers and is fully compatible with Code Composer Studio and all current Windows operating systems. Predator-II is based on the well proven Predator PCMCIA Emulator with improved driver circuits and a new PCMCIA to POD cable to provide greater reliability, low-voltage DSP support with automatic voltage detection circuitry, plus new indicator lights on the POD. Predator-II is the perfect choice for laptop users who are in need of faster program load performances.

FEATURES:

- Fast download speeds for debugging large applications
- Easy portability in the field
- Ideal for handling large programs
- No need for external power
- Operation/Diagnostics via POD LEDs
- PCI carrier card option enables the Predator-II to be used with desktop PCs

For more information, contact: sales@kanecomputing.com

RSC# 31725 @ www.dsp-fpga.com/rsc

SPIRIT DSP
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www.spiritdsp.com

SPIRIT DSP
Embedded Voice Experience

SPIRIT Audio Engine

SPIRIT offers award-winning, field-proven portfolio of multimedia software solutions. SPIRIT Audio Engine is an integrated software suite of carefully optimized audio components for mobile and portable multimedia applications. SPIRIT Audio Engine has been hand-tuned to ensure minimum CPU power consumption and increase battery life in power-sensitive portable applications. It supports the most popular audio formats for playback and recording.

This software suite includes audio codecs (MP3, AAC, WMA, SBC etc.) and must-have audio utilities (parametric equalizer, loudness control, time stretching, LBR recovery and other additional features).

FEATURES:

- Only 10 MHz CPU load while playing back WMA, MP3 and AAC LC streams to ensure maximum battery-life in power-sensitive portable apps
- Small memory footprint for cost-efficient design
- Simple API to facilitate integration and reduce time-to-market
- High sound and image quality even on low-cost devices
- Compliance with open standards
- Complete solution from one source to reduce integration time and effort

For more information, contact: biz@spiritdsp.com **RSC# 31744 @ www.dsp-fpga.com/rsc**

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www.spiritdsp.com

SPIRIT DSP
Embedded Voice Experience

TeamSpirit™ Mobile

TeamSpirit™ Mobile, the world's most compact voice engine, helps mobile OEMs and service providers quickly hit the voice over Wi-Fi market. With a single low-MHz-processor mobile OEMs can open mass market for VoIP-enabled handsets and ensure customers' satisfaction with prolonged battery life. Support for a wide range of mass market handsets allows softphone developers to go mobile and cover plenty of users.

TeamSpirit™ Mobile incorporates the voice processing functionality of a softphone. It integrates network and voice subsystems and ensures the lowest CPU load. TeamSpirit™ Mobile includes a speech codecs' library, speech enhancement algorithms for superior voice quality, and network optimizing functionality to handle varying delay (jitter) and packet loss.

TeamSpirit™

FEATURES:

- Complete voice and video engine for mobile platforms
- Low BOM cost with single low-MHz processor platforms
- Easy integration, fast time-to-market
- Highest voice quality, sophisticated speech enhancement algorithms
- Optimized for dual-mode phones GSM/UMTS/CDMA and Wi-Fi
- Can be enhanced with video support using TeamSpirit™ Video

For more information, contact: biz@spiritdsp.com **RSC# 31743 @ www.dsp-fpga.com/rsc**

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Synplicity®
Simply Better Results

Synplify DSP

Advanced FPGAs are the perfect vehicle for high performance DSP applications. Hundreds of millions operations per second can be achieved, and dedicated DSP blocks and multipliers facilitate efficient and parallel implementation of DSP functions. However the traditional implementation path of hand-coding the RTL often is error-prone and time consuming, with numerous iterations between the algorithm architect and the hardware designer. With Synplify DSP you can model and simulate your algorithms quickly, and automatically create optimized RTL implementations for a wide range of target devices.

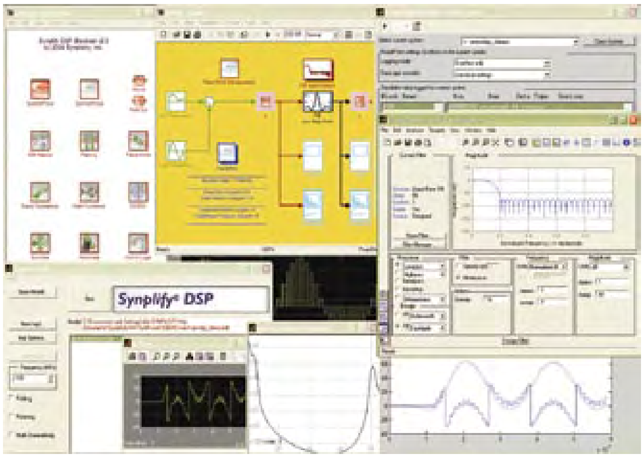
Automated RTL implementation – The Synplify DSP product automatically generates RTL and a verification test bench from a Simulink system-level specification. No hand-coding of any RTL is required.

The Synplify DSP blockset – Synplify DSP provides a set of functional blocks commonly used in DSP design including filtering (FIR, IIR), transforms, math functions, CORDIC, signal operations, memories, and control logic. These functions are technology-independent and tightly integrated into The MathWorks environment, allowing the algorithm designer to utilize Simulink features such as discrete-time simulation, multi-rate management, fixed point quantization, scope debugging, and more.

FPGA hardware independence – Synplify DSP allows algorithm behavior to be captured in Simulink without preselecting the specific FPGA device for implementation. The Synplify DSP toolbox automatically implements an optimized architecture in RTL based upon your timing and area requirements.

Multi-channel system from single-channel specification – Synplify DSP enables quick what-if analysis on channel capacity by automatically generating a pipelined system from a single channel specification.

Area-speed tradeoffs – Math intensive DSP algorithms easily consume large numbers of expensive hardware functions such as multipliers. The Synplify DSP tool analyzes the design to automatically find opportunities for sharing these resources, saving design iterations and significant area.



FEATURES:

- Rapidly create high-level, technology independent DSP models with fully integrated Synplicity fixed-point DSP library
- High quality RTL code and testbench automatically synthesized from Simulink model
- DSP synthesis – DSP architecture optimizations such as system-level re-timing for performance and folding for area utilization
- Extensive floating-point to fixed-point conversion and analysis
- Vector support – concise expression of parallel and multi-channel operations
- Powerful system-wide optimizations for performance, area, and multi-channelization tradeoffs
- Technology independence allows targeting any FPGA architecture from the same Simulink model
- M-control – use a subset of M-language to describe complex state machine and control logic
- Multi-channelization – automatically produces a resource optimized multi-channel implementation from a single channel specification
- Integrated quantization and multi-rate analysis – accelerate design and verification of fixed-point multi-rate DSP algorithms
- Automatic datatype propagation propagates type and adjusts word width to avoid overflow saving manual calculation and implementation
- Synplify DSP blockset – hardware abstraction focuses on algorithm behavior, separates implementation details and enables full portability

For more information, contact: info@synplicity.com

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Nallatech
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Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenBLUE-Virtex 4

Dual Virtex-4 SRAM DIME-II Module

Designed for the most demanding processing applications, the BenBLUE™-V4 is the ideal solution when the highest processing density is required. The BenBLUE-V4 combines two Xilinx Virtex-4 LX FPGAs and 64 MB of DDR-II SRAM in eight independent banks, offering processing and memory expansion capability for Nallatech CompactPCI, VME, PCI, and PCI-104 COTS FPGA computing systems.

The high-bandwidth DDR-II SRAM enables developers to leverage the full processing capability of the onboard Virtex-4 FPGAs for maximum application performance.

This functionality is combined in a proven COTS solution, designed for ease of use, low-risk, and straightforward system integration/in-field deployment in applications including C4ISR and image processing.

FEATURES:

- Two onboard Xilinx Virtex-4 user FPGAs, with two Virtex-4 LX100 or LX160
- Up to 300k+ logic cells per module
- 64 MB DDR-II SRAM – eight independent banks; 16 GBps total DDR-II SRAM bandwidth
- Includes DDR-II SRAM FPGA IP core
- FUSE system software and DIMEtalk design environment compatible
- Multiple design-entry flows supported; also supports industry-standard synthesis and implementation tools

For more information, contact: contact@nallatech.com

RSC# 31737 @ www.dsp-fpga.com/rsc

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www.nallatech.com

BenDATA™-V4

Virtex-4 SRAM/DRAM DIME-II Module

For applications requiring the combined processing capability of very high-bandwidth, high-density external memories and the latest FPGA technology, the BenDATA-V4 is the ideal solution. Combining a Xilinx Virtex-4 SX or LX FPGA, 1 GB DDR2 SDRAM, and 16 MB of DDR-II SRAM, the module provides processing and memory expansion capability. The combination of high-density DDR2 SDRAM and rapid, random-access DDR-II SRAM offers maximum flexibility for application implementation.

This functionality is combined in a proven COTS solution, designed for ease of use, low-risk, and straightforward system integration/in-field deployment applications including SIGINT and C4ISR.

FEATURES:

- DIME-II expansion module
- On-board Xilinx Virtex-4 SX55, LX100 or LX160 user FPGA
- 1 GB DDR2 SDRAM – two independent banks
- 16 MB DDR-II SRAM – two independent banks and eight GBps total SRAM
- Multiple design-entry flows, industry-standard synthesis, and implementation tools supported
- FUSE system software and DIMEtalk design environment compatible

For more information, contact: contact@nallatech.com

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Innovative Integration

2390-A Ward Avenue • Simi Valley, CA 93065
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www.innovative-dsp.com

UWB

The UWB Receiver PMC/XMC card features the most advanced architecture for ultrafast signal capture and real-time processing in wideband radio systems and similar wide spectrum applications. It integrates two 250 MSPS, 12-bit A/D channels with a large FPGA for user code, ample memory, and flexible clocks/triggers on a PMC/XMC mezzanine format. The UWB has a Xilinx Virtex-II Pro FPGA for signal processing that may be quickly customized using Innovative's Framework Logic in VHDL or in the MATLAB Simulink graphical environment. Large on-card memories for data capture and analysis, a flexible clocking structure, and 1 GBps connectivity to host DSP cards make the UWB a powerful front end to many applications.

FEATURES:

- Two LTC2224, 12-bit 250 MSPS converters
- Virtex-II Pro FPGA, 4 million gates
- PCI 64/66 with Pn4 port to host card
- XMC – 1 GBps full-duplex rates per VITA 42
- 64 MB SDRAM plus 2 MB RAM for FPGA
- Sample clocks: Dual external or on-card PLL

For more information, contact: sales@innovative-dsp.com

RSC# 31722 @ www.dsp-fpga.com/rsc

Radstone Sensor Processing

296-300 Concord Road, Corporate Center, Suite 120
Billerica, MA 01821
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www.radstone.com

ICS-7003

The ICS-7003 is a full length PCI card with an x8 PCI Express interface capable of carrying two single-width PCI Mezzanine Card (PMC) modules. Designed to deliver high performance via eight lanes of PCI Express I/O and dual FPDP connectors, the ICS-7003 is the only long format (i.e. dual PMC) PCI Express carrier card yet announced to support this level of functionality. Each of the PMC sites are PCI-X (64-bit, 133 MHz) compliant, and the board includes a PCI Express to dual PCI-X bridge, making it more than capable of fully exploiting the maximum theoretical transfer capability of the two PCI-X modules at the same time – far beyond the capability of any non PCI Express carrier.

FEATURES:

- Adapts two PMC cards to x8 PCI Express interface
- Each PMC site supports PCI-X 133 MHz allowing data rates up to 1 GBps
- Intelligent switch matrix provides user defined Pn4 connections between PMCs, or to FPDP II peripherals
- Transparent installation into PCIe systems – no additional drivers required
- Ideal for real-time applications that need high rate data movement in a PC server or workstation platform

For more information, contact: sales@ics-ltd.com

RSC# 31742 @ www.dsp-fpga.com/rsc

BittWare, Inc.
31B South Main Street • Concord, NH 03301
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www.bittware.com

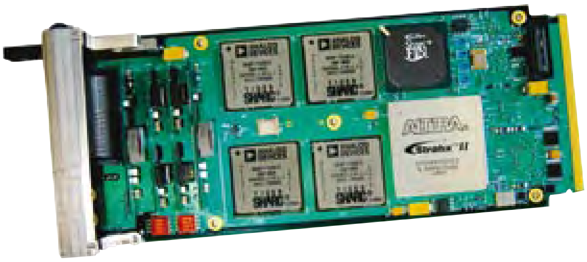
B2-AMC

Featuring Analog Devices' ADSP-TS201S TigerSHARC processor and Altera's Stratix II FPGA, BittWare's B2-AMC (B2AM) is an Advanced Mezzanine Card (AdvancedMC) that supports universal baseband processing for wireless communications infrastructure such as 2G, 2.5G, 3G, WiMAX, and SDR. A full-height, single-wide AdvancedMC, the B2AM attaches to AdvancedTCA carriers or other cards equipped with AdvancedMC bays and is completely hot swappable. The B2AM features a single cluster of four ADSP-TS201S TigerSHARC DSPs from Analog Devices, providing a total of 14.4 GFLOPS floating point and 57.5 GOPS of 16-bit fixed point processing power. In addition to 24 Mb of on-chip RAM, each TigerSHARC also boasts four high speed LVDS link ports at 500 MBps each.

The Altera Stratix II FPGA facilitates off-board I/O and provides communications routing and processing via BittWare's ATLANTiS. ATLANTiS implements eight TigerSHARC link ports, supporting a variety of external I/O, flags, and interrupts, and can be configured to connect any I/O or link port to any other I/O or link port, allowing any combination of inputs and outputs to be routed together. Broadcast, multicast, and dynamic reconfigurability are also supported. ATLANTiS allows designers to route data to internal FPGA processing blocks for pre-, post-, or co-processing.

ATLANTiS interfaces to four ports in the AdvancedMC fat pipes via PMC Sierra's QuadPHY SerDes. The four ports provide a network data and control switch fabric interface on the AdvancedMC connector, configurable to support PCI Express, Advanced Switching Interconnect (ASI), Serial RapidIO, GbE, or XAUI. Alternatively, a single SerDes port can be run via a front panel fiber transceiver. BittWare's SharcFINe Bridge provides Gigabit Ethernet and PCI Express via the common options region. It also provides 10/100 Ethernet and RS-232 on the AdvancedMC front panel.

ATLANTiS provides 11 pairs of LVDS I/O (5 Rx, 1 Rx clk, 5 Tx) for proprietary antenna or network interfaces and 24 bits of general purpose digital I/O available on the AdvancedMC front panel. The B2AM implements the standard IPMI.



FEATURES:

- Full-height, single-wide AdvancedMC
- ADSP-TS201 DSP cluster of 4 ADSP-TS201S TigerSHARC DSPs providing 57.5 GOPS 16-bit fixed point and 14.4 GFLOPS floating point processing power
- BittWare's ATLANTiS implemented in an Altera Stratix II FPGA for I/O, routing, and processing
- Fat pipes and common options interfaces for data and control providing the following:
  - Network interface configurable to support
    - Serial RapidIO
    - PCI Express and ASI
    - GbE, XAUI (10 GbE)
  - SharcFINe bridge providing GbE and PCI Express
  - Module Management Control implementing IPMI
    - Temperature monitoring
    - Hot swap support
    - System synchronization via AdvancedMC systems clocks
- Front panel I/O providing the following:
  - 10/100 Ethernet: LVDS I/O – general purpose digital I/O
  - RS-232: Optional 1x fiber transceiver (replaces AdvancedMC fat pipes) – JTAG port for debug support
- Booting of DSPs and FPGA via flash nonvolatile memory

For more information, contact: info@bittware.com.

RSC# 31708 @ www.dsp-fpga.com/rsc

Improv Systems Inc.
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www.improvsys.com

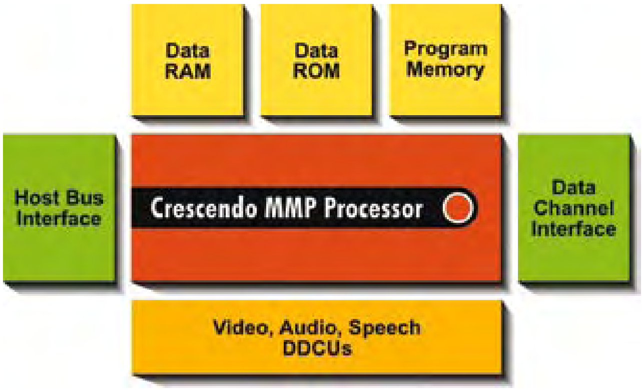
Jazz Media Cores

The Jazz Media cores are highly optimized solutions specifically tailored to the demanding needs of consumer media markets. Whether you are replacing an existing design or adding media processing to your designs, the Jazz cores can get you to market quickly and efficiently. They support a wide range of video, audio, image, and speech standards and are optimized for low power, low cost applications.

New media devices require support for a variety of different video, audio, image, and speech standards. The Jazz Media solutions are delivered with a complete set of media software modules that can be loaded from memory; this allows a single core to support a broad range of media standards. The Jazz Media cores are fully pre-configured and pre-optimized for specific applications. They include built-in interfaces for standard on-chip buses and memory management to allow direct drop-in into an existing SoC architecture. The Jazz Media cores come with sophisticated power management features and multiple power savings modes.

A complete software development environment called the Jazz Standard tool suite supports all the Jazz cores. The cores also come with a complete implementation environment called the Jazz Generator which creates complete RTL, EDA tool scripts, verification environment, and FPGA mapping. Improv also offers a development platform using Improv's FPGA-based Jazz Rehearsal cards with a full test environment to support verification and system integration.

Improv also offers the Jazz Voice cores for voice-over-IP applications and the Jazz DSP family for general-purpose DSP.



FEATURES:

- Complete silicon-ready solution
- Optimized for small die size and low power
- Low clock rates for advanced media standards
- Available in audio, video, and full media configurations
- Video software modules inlcuded with license including H.264, MPEG-4, MPEG-2, WMV, and ON2
- Audio software modules included with license including AAC, MP3, MP L1/L2, Dolby Digital, BSAC, and PCM
- Optional image (JPEG) and speech (G.7xx) software modules available as add-on package
- Complete hardware and solftware solution ready for silicon
- Reduces CPU load by 75-90 percent
- Fully synthesizable and foundry-independent
- Supported by a comprehensive software development tool suite
- Optionally available as configurable cores for additional customization

For more information, contact: caryu@improvsys.com

RSC# 31716 @ www.dsp-fpga.com/rsc

Tundra Semiconductor

603 March Road • Ottawa, ON K2K 2M5 Canada
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www.tundra.com

Tundra Tsi578

The Tsi578™ serial RapidIO® switch sets industry benchmarks for high-performance and low power consumption through an innovative feature set. It supports RapidIO version 1.3 and is ideally suited for AdvancedTCA® and MicroTCA™ backplane or local DSP connectivity. These platforms will benefit from the switch's ability to route packets to more than 64,000 endpoints, independent unicast and multicast routing mechanisms, and error management extensions. Scalable for a broad spectrum of wireless, networking, and video infrastructure applications, designers can take advantage of configuration options to efficiently manage power requirements for high-performance.

FEATURES:

- Supports 80 Gbps aggregate bandwidth
- Up to eight 4x mode ports or sixteen 1x mode ports
- Port frequency configuration to 1.25, 2.5, and 3.125 Gbps with 8 b/10 b encoding
- Integrated high-speed, full-duplex SERDES with 200 mW per port power
- High-performance hardware multicast
- Advanced traffic management features

For more information, contact: sales@tundra.com

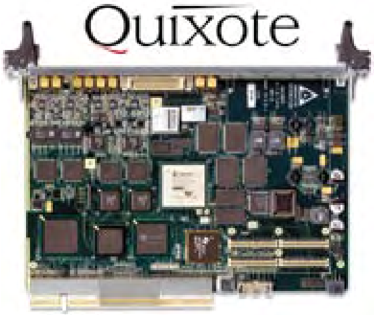
RSC# 31757 @ www.dsp-fpga.com/rsc

Innovative Integration

2390-A Ward Avenue • Simi Valley, CA 93065
Tel: 805-578-4260 • Fax: 805-578-4225
www.innovative-dsp.com

Quixote

Quixote is a 64-bit CompactPCI 6U board for advanced signal capture, generation, and coprocessing. It combines one C6416 DSP with a two- or six- million-gate Virtex-II FPGA, utilizing the best of both worlds in signal processing technology to provide extreme processing flexibility and efficiency and deliver unmatched performance. Dual 105 MHz analog inputs/outputs integrate signal capture and waveform generation right on the FPGA external interface. One PMC site facilitates integration of off-the-shelf or custom PMC mezzanine boards. PCI-to-StarFabric bridge offers two 2.5 Gbps ports to the new PICMG 2.17 switched interconnect backplane.



FEATURES:

- 1 GHz TMS320C6416 DSP
- 2-6 MGATE Virtex-II FPGA
- 32 MB SDRAM, 8 MB ZBT SBSRAM
- AD6645 & AD9764 converters
- 64/32-bit CompactPCI, 66 MHz, 5 V/3.3 V
- Complex trigger modes with HW event logging

For more information, contact: sales@ innovative-dsp.com

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Traquair Data Systems, Inc.
114 Sheldon Rd • Ithaca, NY 14850
Tel: 607-266-6000 • Fax: 607-266-8221
www.traquair.com

micro-line C641x DSP/FPGA Boards

The micro-line series of embedded DSP/FPGA boards provide embedded systems developers with a tightly integrated suite of programmable DSP, FPGA, and I/O resources in small, stand-alone capable board formats.

micro-line C641xCPU and C6412Compact DSP/FPGA boards target high-performance integer DSP applications, using the powerful Texas Instruments TMS320C641x DSP processors.

The C641xCPU boards incorporate either a 400 MHz TMS320C6410, a 500 MHz TMS320C6413 or 500 MHz TMS320C6418 integer DSP, with up to 64 MB SDRAM, 8 MB boot program FLASH ROM, and on-board, high-density 500 KGate, 1 MGate, or 1.6 MGate Spartan-3E FPGA. The Spartan-3E is optionally programmable and offers developers the means to complement the resources of the DSP with FPGA-based DSP algorithms as well as configurable digital I/O capabilities.

For more demanding applications, the C6412Compact combines a more powerful 720 MHz TMS320C6412 DSP with up to 128 MB SDRAM, up to 16 MB boot program FLASH ROM, a high-density 1 MGate or 4 MGate Spartan-3 FPGA, an on-board USB 2.0 slave interface, an 10/100BaseTx Ethernet interface, and two independent 1394a FireWire interfaces. The C6412Compact also offers a 32-bit 33/66 MHz PCI interface and 64-bit bus width connecting the DSP, FPGA, SDRAM, and FireWire interfaces.

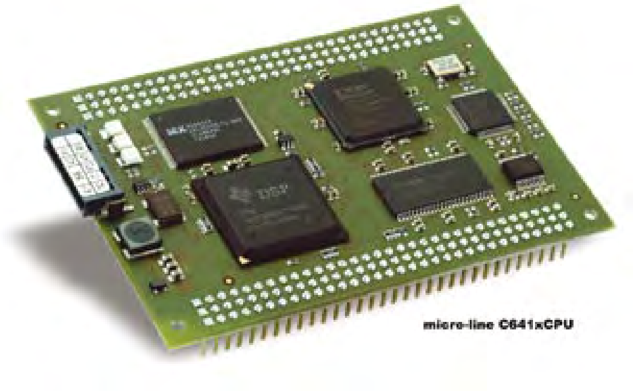
10/100BaseTx Ethernet support is optionally available using Windmill Innovations' eXpressDSP-compliant bf3Net TCP/IP protocol stack and bf3Web embedded web server (requires SC100BaseTx Ethernet daughtercard when using C641xCPU boards).

Optional Analog I/O daughtercards can also be used with the C641xCPU and C6412Compact boards:

ORS-112 (16-bit A/D/A)
  – 4-ch A/D 2.5 MSps; 4-ch D/A 625 KSps

ORS-114 (14-bit A/D/A)
  – 2-ch A/D 65 MSps; 2-ch D/A 125 MSps

ORS-116 (16-bit A/D/A)
  – 12-ch A/D 250 KSps; 12-ch D/A 100 KSps


micro-line C641xCPU

FEATURES:

- C641xCPU
  - 400 MHz TMS320C6410, or 500 MHz TMS320C6413, or 500 MHz TMS320C6418 integer DSP
  - 500 KGate, 1.2 MGate, or 1.6 MGate Xilinx Spartan-3E FPGA; up to 98 configurable digital I/O pins
  - Up to 64 MB SDRAM; 8 MB boot program FLASH ROM
  - RS-232 interface
  - 98 mm x 67 mm footprint; ISO9001:2000 accredited production and CE certification
- C6412Compact
  - 720 MHz TMS320C6412 integer DSP
  - 1 MGate or 4 MGate Spartan-3 FPGA
  - Up to 128 MB SDRAM; up to 16 MB boot program FLASH ROM
  - USB 2.0 slave interface
  - Two independent IEEE1394a FireWire interfaces for streaming data in/out simultaneously
  - 16-/32-bit host port interface or 32-bit 33/66 MHz PCI bus
  - RS-232 interface

For more information, contact: sales@traquair.com **RSC# 31755 @ www.dsp-fpga.com/rsc**

Traquair Data Systems, Inc.
114 Sheldon Rd • Ithaca, NY 14850
Tel: 607-266-6000 • Fax: 607-266-8221
www.traquair.com

micro-line C6713 DSP/FPGA Boards

The micro-line series of embedded DSP/FPGA boards provide embedded systems developers with a tightly integrated suite of programmable DSP, FPGA, and I/O resources in small, stand-alone capable board formats.

micro-line C6713Compact and C6713CPU DSP/FPGA boards target high-performance floating-point DSP applications, using the powerful Texas Instruments TMS320C6713 DSP processor.

The C6713Compact incorporates up to 64 MB SDRAM, 8 MB boot program FLASH ROM, and an on-board, high-density 250 kGate, 500 kGate, or 1 MGate Virtex -II FPGA (optionally programmable). The FPGA greatly expands processing as well as hardware interfacing possibilities. A 400 Mbps IEEE1394a FireWire interface is also included on-board, for communications with other embedded DSP resources, cameras, sensors, and PCs. Software APIs are available to utilize the FireWire interface for general purposes, video frame capture from cameras, and data storage to hard drives and CompactFlash memory.

The C6713CPU offers a smaller (98 mm x 67 mm footprint) and leaner configuration, with up to 64 MB SDRAM, 2 MB boot program FLASH ROM, and a high-density 400 kGate or 1 MGate Spartan-3 FPGA.

10/100BaseTx Ethernet support is optionally available using Windmill Innovations' eXpressDSP-compliant bf3Net TCP/IP protocol stack and bf3Web embedded web server (requires SC100BaseTx Ethernet daughtercard).

Optional Analog I/O daughtercards can also be used with the C641xCPU and C6412Compact boards:

ORS-112 (16-bit A/D/A)
  – 4-ch A/D 2.5 MSps; 4-ch D/A 625 KSps

ORS-114 (14-bit A/D/A)
  – 2-ch A/D 65 MSps; 2-ch D/A 125 MSps

ORS-116 (16-bit A/D/A)
  – 12-ch A/D 250 KSps; 12-ch D/A 100 KSps

micro-line C6713Compact

FEATURES:

- C6713Compact
  - 225 or 300 MHz TMS320C6713 floating-point DSP
  - 250 KGate, 500 KGate, or 1 MGate Virtex-II FPGA; up to 160 configurable digital I/O pins
  - Up to 64 MB SDRAM; 8 MB boot program FLASH ROM
  - On-board 400 Mbps IEEE1394a FireWire interface
  - RS-232 interface
  - External access to TMS320C6713 DSP I/O interfaces: 32-bit EMIF, XF0/1 pins, Timer input/output pins, McASP and McBSP ports, I^{2}C, and HPI
  - 67 mm x 120 mm footprint; ISO9001:2000 accredited production and CE certification
- C6713CPU
  - 300 MHz TMS320C6713 floating-point DSP
  - 400 KGate or 1 MGate Spartan-3 FPGA
  - 64 MB SDRAM; 2 MB boot program FLASH ROM
  - RS-232 interface
  - 98 mm x 67 mm footprint; ISO9001:2000 accredited production and CE certification

For more information, contact: sales@traquair.com

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Embedded

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Innovative Integration

2390-A Ward Avenue • Simi Valley, CA 93065
Tel: 805-578-4260 • Fax: 805-578-4225
www.innovative-dsp.com

SBC6713e

SBC6713e is a high-performance, flexible, standalone DSP board with Ethernet connectivity, loaded with I/O peripherals. Built around the powerful, C-friendly, 300 MHz floating-point C6713 DSP, it is a fully open platform with 15+ off-the-shelf OMNIBUS I/O modules available that provide a wide choice of A/D and D/A and also support simple EMIF bus interface to custom I/O daughter cards. TCP/IP is running on a dedicated DM642 coprocessor to preserve the C6713 for user code and other peripheral controls. System-level integration is facilitated with onboard digital I/O, DDS time base, external clock input, multicard sync, FPDP port data links, 2 MB flash ROM, and watchdog.

FEATURES:

- 300 MHz TMS320C6713 DSP (floating point)
- Two OMNIBUS I/O expansion sites
- 10/100 Ethernet, RS-232 port
- FPDP data port to 200 MBps
- Capable of 100 percent standalone operation
- 600 Kgate Spartan-IIE for user code (optional)

For more information, contact: sales@innovative-dsp.com

RSC# 31723 @ www.dsp-fpga.com/rsc

Proprietary

DSP-FPGA.com Resource Guide 2006

Hunt Engineering

Burton Row • Brent Knoll, Somerset, TA9 4BP United Kingdom
Tel: +44 (0)1278 760188 • Fax: +44 (0)1278 760199
www.hunt-dsp.com

HERON FPGA and DSP

HERON high-performance, modular systems, designed for real-time, are programmable and reconfigurable, using common APIs for compatibility and complete flexibility. Systems can be used connected to a PC or standalone. Use modules with Virtex-II, II Pro and Virtex-4 Xilinx FPGA, TI DSP and powerful I/O modules in any combination. Some FPGA modules have embedded PowerPC and/or external SDRAM.

Mount the modules on a HERON module carrier providing many real-time data connections at up to 400 MBps in each direction simultaneously. Scale from a single module embedded system to an extensible multi-carrier system using interboard connection modules.

Program the system using the system tools, examples, tutorials, IP for commonly used functions which are included

PCI, USB and CompactPCI Module Carrier Boards
Modules with FPGA and fast I/O
Modules with C6000 DSP
Modules for connecting Carrier Boards together
Modules with I/O only

FEATURES:

- Xilinx Virtex-II and II Pro,Virtex-4 FPGA, 1-8 M gates, optional SDRAM, programmable I/Os and embedded PowerPC
- C6x DSP modules with 2,400 MIPS, SDRAM, Flash-ROM, I/Os
- Modules with FPGA plus two channels each of 210 MSps A/D and 160 MSps D/A
- Carriers with 1-4 slots available for CompactPCI, PCI, USB, and embedded/standalone use
- Real-time data connections at up to 400 MBps in each direction simultaneously
- System development tools, IP, software demos, examples and tutorials included, free technical support

For more information, contact: sales@hunteng.co.uk

RSC# 31715 @ www.dsp-fpga.com/rsc

Danville Signal Processing, Inc.
38570 100th Avenue • Cannon Falls, MN 55009
Tel: 507-263-5854 • Fax: 877-230-5629
www.danvillesignal.com

SHARC DSP boards

Danville's SHARC-based dspstak and dspblok families simplify DSP-based embedded applications using the latest Analog Devices SHARC DSPs.

Each dspstak consists of a DSP engine and one or more I/O modules. A dspstak DSP engine consists of a SHARC, Flash and EE memory, programmable clocks, and RS-232 and USB interfaces. There are dspstak boards that include an Analog Devices onboard debugger (ICE). These boards emulate an Analog Devices EZ-KIT and, at the same time, create production-ready, off-the-shelf solutions.

Danville's dspblok DSP modules are small plug-ins (60 mm x 60 mm) that allow DSP functionality to be easily added to your product.

FEATURES:

- Analog Devices ADSP-21369 and ADSP-21262 SHARC DSPs
- Supported by Analog Devices Visual DSP 4.5++ including EZ-KIT version
- USB 2.0 interface with Device Driver support
- Code examples and libraries for easy software development
- Field reprogrammable via USB or RS-232
- Separate I/O modules allow flexible configurations

For more information, contact: dspfpga@ danvillesignal.com RSC# 31712 @ www.dsp-fpga.com/rsc

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Nallatech
1010 Liberty Road, Suite 103 • Eldersberg, MD 21784
Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenONE-PCI-104

The BenONE-PCI-104 FPGA computing card brings the processing power of FPGAs to the popular, compact PCI-104 form factor, providing a powerful platform for high-performance systems development and deployment in production environments. Using DIME-II expansion modules, the BenONE-PCI-104 supports Virtex-4, Virtex-II Pro, and Virtex-II FPGAs, complemented by a selection of memory and analog and digital I/O interfaces. The BenONE-PCI-104 FPGA computing card provides a powerful platform for embedded systems development and deployment in production environments. Combined with DIMEtalk for easy connectivity implementation and FUSE for host integration, the BenONE-PCI-104 offers a professional, compact, and standalone platform for embedded deployment applications.

FEATURES:

- PCI-104 form factor
- Single DIME-II module expansion slot
- Xilinx Virtex-4 and Virtex-II Pro supported through DIME-II expansion modules
- 32-bit, 33 MHz PCI interface
- Digital I/O header
- Windows and Linux support (VxWorks on request); includes FUSE FPGA Computing Runtime Software

For more information, contact: contact@nallatech.com RSC# 31734 @ www.dsp-fpga.com/rsc

Synplicity, Inc.

600 West California Avenue • Sunnyvale, CA 94086
Tel: 408-215-6000 • Fax: 408-222-0263
www.synplicity.com

Synplify Pro

The Synplify Pro product achieves industry-leading QoR by incorporating several advanced optimization techniques including Synplicity's proprietary Behavior Extracting Synthesis Technology (BEST). By extracting behavior such as Finite State Machines (FSM), multipliers, and memories from RTL code and starting synthesis at this level, the Synplify Pro product optimizes your design globally for improved performance and at the same time can run faster and handle larger designs than alternative synthesis tools. Another important technique for improved performance is retiming. By selecting a switch, you can tell the tool to automatically move registers inside combinatorial logic in order to balance timing delay and improve circuit performance by as much as 20 percent. Retiming may be used on a global level or selectively.

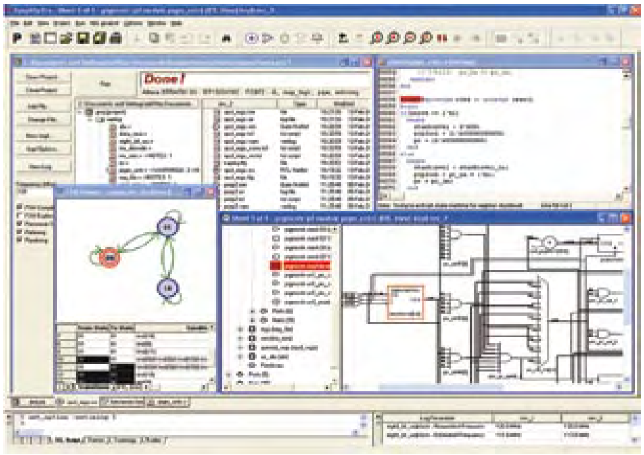
The HDL Analyst RTL graphical analysis and debugging tool provides instant graphical views of both high-level block diagrams and gate-level schematics linking back to the RTL source code, making debug and code optimization fast and easy. Critical paths of your design are quickly highlighted and linked back to your RTL source.

The FSM Explorer automatically finds state machines in your design, then evaluates alternative encoding styles and selects the one giving the best solution for the specified timing constraints. FSMs are displayed as bubble diagrams, providing an easy-to-read graphical representation of your results.

Synplicity's MultiPoint synthesis technology provides a unique and superior approach to incremental design. User-defined compile points and intelligent, difference-based synthesis technology provides a high level of design stability for incremental changes without the performance penalty of other incremental design styles.

The Synplify Pro solution offers a formal verification mode where optimizations are recorded and passed on to tools such as Cadence's Conformal product for this purpose.

The Synplify Pro tool interfaces to popular HDL simulators and is tightly integrated with place and route tools from Actel, Altera, Lattice, QuickLogic, and Xilinx.



FEATURES:

- Technology independence – target all popular FPGAs from one RTL and constraint source
- Proprietary BEST algorithms – globally optimized designs in a fraction of the time required by traditional synthesis tools
- True timing-driven synthesis – after meeting timing constraints automatically optimizes for area/cost
- Comprehensive language support – supports Verilog, VHDL, System Verilog, and mixed-language designs
- Automatic RAM inferencing – bypass tedious hand instantiation of RAM
- Lightning-fast compile times – synthesizes even the largest design in minutes
- Automatic retiming – moves registers automatically within combinatorial logic to balance delay and improve performance
- Pipelined multipliers and ROMs – automatic register balancing of pipelined multipliers and ROMs for faster circuit performance
- FSM Explorer – automatically finds and selects the best coding style option for the fastest performance
- Graphical state machine viewer – fast debugging and documentation for all state machines in your design
- HDL analyst RTL analysis and debugging tool – instantly generates an RTL block diagram from HDL code; helps identify critical paths
- MultiPoint synthesis – provides a superior methodology for incremental design

For more information, contact: info@synplicity.com

RSC# 31751 @ www.dsp-fpga.com/rsc

Xilinx
2100 Logic Drive • San Jose, CA 95124
Tel: 408-559-7778 • Fax: 408-559-7114
www.xilinx.com/dsp

XtremeDSP Devices

Xilinx FPGAs are ideal for replacing your ASIC/ASSP or boosting the performance of your DSP processor.

Virtex-4 and Virtex-5 FPGAs series for DSP
Virtex™-4 and Virtex-5 FPGAs deliver the industry's highest performance and lowest power and cost for that performance. They are commonly used for radio-card and baseband co-processing functions in wireless infrastructure, MILCOM, and compute-intensive video imaging applications.

Highest performance: XtremeDSP Slices in Virtex-4 FPGAs deliver up to 256 GMACs performance using 512, dedicated 18 x 18-bit multipliers/48-bit adders, each capable of operating at 500 MHz (DSP48). Virtex-5 devices feature 18 x 25 multipliers/48 bit adders for extended dynamic range and can operate to 550 MHz (DSP48E).

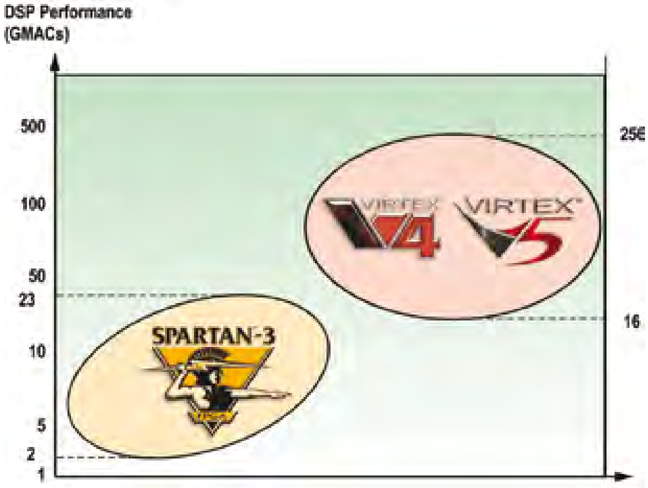
Lowest power: With a power consumption of only 1.38 mW/100 MHz per DSP48E, Virtex-5 FPGAs enable you to significantly reduce the power per channel in your communications or video systems.

Lowest cost for highest performance: The Virtex-4 SX platform delivers as many as 512, 500 MHz XtremeDSP Slices in a device that consumes half the silicon area of competing FPGAs. The Virtex-5 LX platform delivers up to 192 DSP48E slices.

Spartan 3/3E FPGAs for DSP
Starting at only $2 for 100 K gates, Spartan™-3/3E FPGAs are ideally suited for compute-intensive applications where GMACs per dollar is important. Spartan-3/3E FPGAs enable you to build parallel DSP structures using 104, 18 x 18 embedded multipliers. Spartan-3/3E FPGAs are ideal for high-volume consumer and automotive applications.

In addition to signal processing, Virtex-4 and Spartan-3/3E FPGAs are ideal for lowering your system cost (through consolidating your system logic), bridging your serial or parallel buses, and implementing low-rate control functions using on-chip microprocessors such as IBM PowerPC™, Xilinx MicroBlaze™, and PicoBlaze™. For information about Xilinx XtremeDSP Development Tools, see the Software section in this resource guide.

Visit www.xilinx.com/dsp for more information.



FEATURES:

- Virtex-5 FPGAs for extended dynamic range (18 X 25 multiply 48-bit add) and 550 MHz performance
- Virtex-4 FPGAs feature up to 512, 500 MHz (DSP48) XtremeDSP Slices (18 x 18 multiply, 48-bit add)
- Virtex-5 for lowest power per channel – each DSP48E Slice consumes only 1.38 mW per 100 MHz
- Spartan-3/3E for lowest cost FPGA-based DSP – Prices starting at $2 for 100 k gates in big volumes
- Spartan-3/3E for DSP performance acceleration in consumer/automotive applications – Up to 104, (18 x 18) 200+ MHz 18 x 18 multipliers
- XtremeDSP development tools cater to hardware and non-hardware designers that prefer to use MATLAB/Simulink
- More than 60 XtremeDSP algorithms available from Xilinx and partners to help you finish first
- Multiple XtremeDSP development platforms available for standalone FPGA design or DSP co-processing
- XtremeDSP education classes help you become proficient in the XtremeDSP design flow and design implementation techniques
- Award-winning technical support

For more information, contact: narinder.lall@xilinx.com

RSC# 31772 @ www.dsp-fpga.com/rsc

Lattice Semiconductor
5555 NE Moore Ct. • Hillsboro, OR 97124
Tel: 503-268-8000 • Fax: 503-268-8347
www.latticesemi.com

LatticeECP2 FPGAs

The LatticeECP2 (EConomy Plus 2nd generation) family redefines the low-cost FPGA category. By integrating features and capabilities previously only available on higher cost, high-performance FPGAs, this family dramatically expands the range of applications that can take advantage of low-cost FPGA products.

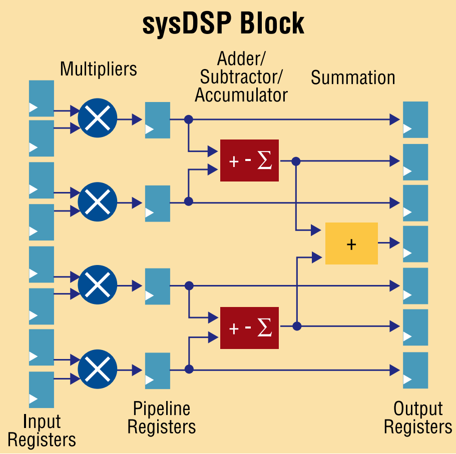
Features that the LatticeECP2 family brings to the low-cost FPGA category include high-performance DSP blocks, up to 70K LUT capacity, support for DDR1/2 memory interfaces at 400 MBps and up to 840 MBps generic LVDS performance. The LatticeECP2 also provides enhanced FPGA configuration options with features such as dual boot, bitstream encryption, and TransFR I/O capability.

LatticeECP2 FPGA devices include between three and 22 sysDSP blocks. sysDSP blocks support four functional elements in three data path widths: 9, 18, and 36. The resources in each sysDSP block can be configured to support the following four elements: MULT, MAC, MULTADD, and MULTADDSUM.

The number of elements available in each block depends upon the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP. Each sysDSP block can be clocked at 325 MHz yielding a total DSP capability of up to 28,600 Million Multiply Accumulates per second (MMACs)!

ispLeverCORE Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used DSP functions, including: FIR Complier, FFT Complier, NCO, Reed Solomon Encoder/Decoder, Viterbi Decoder, Convolutional Encoder, and more. Go to www.latticesemi.com/products/intellectualproperty for a complete listing of IP.



FEATURES:

- Low-cost FPGA optimized for mainstream applications
- Up to 22 high-performance sysDSP blocks per device
- sysDSP blocks are optimized for processing intensive applications and allow designers to quickly implement DSP functions
- sysDSP blocks provide configurable multiplier widths: one 36 x 36, four 18 x 18, eight 9 x 9
- sysDSP blocks provide programmable addition, subtraction, and accumulate modes
- sysDSP blocks offer programmable pipelining – input, intermediate, and output
- One LatticeECP2 device can provide up to 28,600 Million Multiply Accumulates per second (MMACs)
- LatticeECP2 FPGAs support an extensive IP portfolio
- Support for Matlab/Simulink software

For more information, contact: sales@latticesemi.com

RSC# 31726 @ www.dsp-fpga.com/rsc

Nallatech
1010 Liberty Road, Suite 103 • Eldersburg, MD 21784
Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenADC-V4

Virtex-4 / Quad 250 MSps Analog Capture Module

The BenADC-V4 is suitable for applications requiring high-speed analog capture and the processing performance of an on-board FPGA. Combining a Xilinx Virtex-4 SX or LX FPGA, four high speed analog capture channels and two banks of DDR-II SRAM, the module provides processing, analog I/O, and memory expansion capability. The high density of processing and analog capture enables systems to be implemented in less space and makes design implementation easier. This functionality is combined in a proven COTS solutions, designed for ease of use, low risk and straightforward systems integration/in-field deployment.

FEATURES:

- DIME-II expansion module
- On-board Virtex-4 LX100, LX160 or SX55 user FPGA
- Quad 12-bit 250 PSps analog capture channels
- 16 MB DDR-II SRAM, two independent banks
- High memory bandwidth supports double buffering schemes for ADC data capture and processing
- Includes DDR-II SRAM FPGA IP core

For more information, contact: contact@nallatech.com

RSC# 31733 @ www.dsp-fpga.com/rsc

Nallatech
1010 Liberty Road • Eldersburg, MD 21784
Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenADDA-V4

Virtex-4, Dual 105 MSps ADC, Dual 160 MSps DAC DIME-II Module

The BenADDA-V4 is suited for applications requiring high-speed analog capture and the processing performance of an on-board FPGA. Combining a Xilinx Virtex-4 SX or LX FPGA, two analog input channels, two analog output channels, and two banks of DDR-II SRAM, the module provides processing, analog I/O, and memory expansion capability. The high density and direct coupling of processing, memory and analog I/O capability enables systems to be implemented in less space and makes design implementation easier.

FEATURES:

- DIME-II expansion module
- On-board Xilinx Virtex-4 SX55, LX100 or LX160 user FPGA
- Two ADC channels – 14-bits @ 105 MSps
- Two DAC channels – 14-bits @ 160 MSps
- 16 MB DDR-II SRAM – two independent banks
- IP cores for ADC/DAC interfaces and DDR-II SRAM

For more information, contact: contact@nallatech.com

RSC# 31732 @ www.dsp-fpga.com/rsc

Nallatech
1010 Liberty Park Way, Suite 103 • Eldersburg, MD 21784
Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenERA

6U cPCI FPGA Computing Card

The BenERA FPGA computing card provides a powerful platform for high-performance systems development and deployment in production environments. With four DIME-II expansion modules, the BenERA can support combinations of multiple analog and digital I/O interfaces, memory types and up to nine user FPGAs on a single CompactPCI card. Combined with DIMEtalk for easy connectivity implementation and FUSE for host integration, the BenERA offers a professional, easy to use, and low risk solution for a range of end markets.

FEATURES:

- 6U CompactPCI form factor
- 64-bit / 33 MHz PCI interface
- Four DIME-II module expansion slots
- On-board Xilinx Virtex-E user FPGA
- Xilinx Virtex-4 and Virtex-II Pro supported on DIME-II modules
- High bandwidth 240-way backplane GPIO bus

For more information, contact: contact@nallatech.com

RSC# 31731 @ www.dsp-fpga.com/rsc

Nallatech
1010 Liberty Road, Suite 103 • Eldersburg, MD 21784
Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenIO-V4

Virtex-4, SRAM and Digital IO Module

For applications requiring the capability of high bandwidth, high speed external digital I/O and SRAM memory combined with the latest FPGA technology, the BenIO-V4 is the ideal solution. Combining a Xilinx Virtex-4 SX or LX FPGA, 16 MB of DDR-II SRAM and up to 152 digital I/O lines, the module provides I/O, processing and memory expansion capability for the Nallatech CompactPCI, VME, PCI, and PCI-104 COTS FPGA computing systems. This functionality is combined in a proven COTS solution, designed for ease of use, low risk, and straightforward system integration/in-field deployment.

FEATURES:

- DIME-II expansion module
- On board Virtex-4 SX55, LX100 or LX160 user FPGA
- Up to 152 digital I/O lines – configured single-ended or differential operation
- 16 MB DDR-II SRAM – Two independent banks
- Four GBps total SRAM memory bandwidth
- Includes SRAM FPGA cores

For more information, contact: contact@nallatech.com

RSC# 31730 @ www.dsp-fpga.com/rsc

Nallatech
1010 LIberty Park Road, Suite 103 • Eldersburg, MD 21784
Tel: 410-552-3353 • Fax: 410-552-3354
www.nallatech.com

BenNUEY-PCI-104-V4

PCI-104 FPGA Computing Processor Card

The BenNUEY-PCI-104-V4 FPGA computing stack provides a powerful platform for high-performance embedded systems development and deployment in production environments across a variety of applications including signals intelligence, avionics, Software Defined Radio, and autonomous vehicles. This solution is suitable for Size, Weight, and Power (SWAP) constrained real time embedded applications. An on-board Virtex-4 FX FPGA provides the ideal balance of resources for processing and system management, whilst three DIME-II expansion slots allow users to optimize system resources to meet processing, memory, and I/O requirements. The BenNUEY-PCI-104-V4 can support multiple analog and digital I/O interfaces up to seven user FPGAs.

FEATURES:

- PCI-104 form factor
- On-board Xilinx Virtex-4 FX60 or FX100 user FPGA
- 8 MB DDR-II SRAM
- 32-bit / 33 MHz PCI interface
- Three DIME-II module expansion slots
- 100 digital I/O lines – configured single-ended or differential operation

For more information, contact: contact@nallatech.com

RSC# 31729 @ www.dsp-fpga.com/rsc

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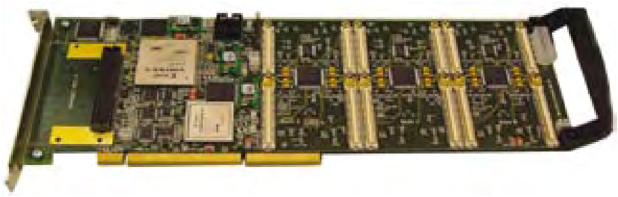
BenNUEY-PCI-X



The BenNUEY-PCI-X FPGA computing card provides a powerful platform for high-performance systems development and deployment in production environments across a variety of applications, including SIGnals INTelligence (SIGINT) and Software-Defined Radio (SDR). An onboard Virtex-4 FX FPGA provides the ideal balance of resources for processing and system management, while three DIME-II expansion slots allow users to optimize system resources to meet processing, memory, and I/O requirements. The BenNUEY-PCI-X can support multiple analog and digital I/O interfaces, memory types, and up to seven user FPGAs on a single PCI-X card. Applications requiring data storage benefit from 18 MB of DDR-II SRAM connected to the Virtex-4 FX user FPGA.

FEATURES:

- PCI-X form factor
- Three DIME-II module expansion slots with onboard Xilinx Virtex-4 FX user FPGA options of XC4VFX60 or XC4VFX100
- 64-bit, 133 MHz PCI-X interface
- 8 MB DDR-II SRAM
- Xilinx Virtex-4-II Pro/-II supported on DIME-II modules
- Windows and Linux support; includes FUSE FPGA Computing Runtime Software

For more information, contact: contact@nallatech.com

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NALLATECH
The High Performance FPGA Solutions Company

BenNUEY-VME64-VXS

6U VME64-VXS FPGA Computing Card

The BenNUEY-VME64-VXS FPGA computing card provides a powerful platform for high-performance systems development and deployment in production environments. Using DIME-II expansion modules, the BenNUEY-VME64-VXS can support multiple analog and digital I/O interfaces, memory types, and up to seven user FPGAs on a single VME card.

FEATURES:

- VME-64-VXS form factor
- Three DIME-II expansion slots
- On-board Xilinx Virtex-II Pro (XC2VP50-6) FPGA available exclusively for user applications
- 8 MB on-board ZBT SRAM 2x SFP I/O ports
- Includes ZBT SRAM interfacing core
- SFP optical connectors on front panel

For more information, contact: contact@nallatech.com

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RADSTONE
SENSOR PROCESSING

ICS-8550

Designed to bring more bandwidth and processing power to Software Defined Radio applications, the ICS-8550 XMC module features two analog inputs equipped with AD9430 210 MHz, 12-bit ADCs, and a Xilinx Virtex-4 XC4VFX60 FPGA. This card has been optimized for wide bandwidth front-end digital signal processing associated with digital receiver applications common to spectrum monitoring, signal intelligence, communications, and radar systems.

Five levels of ruggedization are available from commercial air-cooled to conduction-cooled. Careful selection of components and thermal management techniques allows intensive DSP functionality to be maintained at sample rates up to 210 MHz.

FEATURES:

- Two ADC channels (Analog Devices AD9430): 12-bits @ 210 MHz
- Xilinx Virtex-4 FX60 FPGA
- High-speed serial I/O through XMC connector
- Companion to Radstone V4DSP
- VITA 42 XMC compliant high-speed serial links (eight lanes @ 2.5 GHz)
- Windows, Linux, and VxWorks device drivers with extensive application and technical support available

For more information, contact: sales@ics-ltd.com

RSC# 31741 @ www.dsp-fpga.com/rsc

Annapolis Micro Systems, Inc.
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Dual 2.3 GSps DAC

Annapolis Micro Systems, Inc. is a world leader in high-performance COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing intensive applications.

The Annapolis Dual 2.3 GSps DAC I/O card provides two 12-bit output streams at up to 2.3 GSps per stream.

The board has both a high-precision trigger for inner-board or board-to-board synchronization and a low-precision trigger. The card supports three modes: NRZ, RF, and RZ.

The Xilinx Virtex-II Pro 70 on the board provides user-configurable, real-time continuous sustained processing of the full data stream. Up to two of these I/O cards can reside on the Annapolis WILDSTAR II or WILDSTAR II Pro FPGA-based VME and PCI bus boards, which provide up to 30 million user-reprogrammable FPGA gates for onboard processing. Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. A VHDL source is provided for interfaces to SRAM, LAD bus, I/O bus, and DACs. CoreFire users will have the usual CoreFire board support package.

Develop applications with CoreFire (more than 1,000 cores), which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field. The combination of our COTS hardware and CoreFire enables our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional customer support.

FEATURES:

- Choice of up to 2.3 GSps or 1.5 GSps output per channel
- Two individually configurable output streams of 12-bit data
- High output power and exceptional gain
- Flatness in multiple Nyquist zones
- One Xilinx Virtex-II Pro 70-5, -6, or -7
- Up to 1 GB DDR SDRAM in four banks
- Supports three modes: NRZ, RF, and NZ
- Both high-precision and low-precision triggers
- JTAG and serial port access
- Proactive thermal management system
- Available in both commercial and industrial temperature grades
- Includes one year hardware warranty, software updates, and customer support

For more information, contact: jdonald@annapmicro.com

RSC# 30045 @ www.dsp-fpga.com/rsc

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Tri XFP I/O Card

Annapolis Micro Systems, Inc. is a world leader in high-performance Commercial Off-the-Shelf FPGA-based processing for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing, and other processing intensive applications.

The Annapolis Tri XFP I/O Card, which works with the WILDSTAR 4/5 Family Architecture, has three 10 Gb individually configured XFP connectors, each with its own XAUI to XFI converter. Industry-standard pluggable fiber optic transceivers can be purchased from Annapolis or from other vendors. The Tri XFP provides up to 30 Gb Full Duplex I/O directly between the outside world and the Rocket I/O pins on the Xilinx Virtex-II Pro or Virtex-4 I/O FPGA on the WILDSTAR 4 main board. No other vendor provides that volume of data straight into the heart of the processing elements and then back out again.

Two I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VXS or PCI-X/E board, with up to 30 million user reprogrammable gates.

The Tri XFP card will support 10 Gb Ethernet, 10 Gb Fibre Channel, and OC 192. Although the protocols will be provided as black box solutions with few modifications by users allowed, more adventurous users who choose to develop their own communications protocols from the basics already have access to all the board resources through VHDL source for the interfaces to SRAM, signal conditioners, LAD bus, I/O bus, and PPC flash. CoreFire users will have the usual CoreFire board support package.

The Tri XFP is the first of many I/O cards Annapolis will be releasing for its new WILDSTAR 4/5 Architecture Family, which uses Xilinx Virtex-4 and Virtex-5 FPGAs for processing elements. WILDSTAR 4 is the 10th generation of Xilinx FPGA processing-based COTS boards from Annapolis.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional customer support.

FEATURES:

- Up to 10 Gb Full Duplex Ethernet per connector
- Up to 10 Gb Fibre Channel
- OC 192
- Three 10 Gb XFP connector
- Accepts industry-standard pluggable transceivers
- Available in both commercial and industrial temperature grades
- Includes one year hardware warranty, software updates, and customer support
- One or two I/O cards fit on a single WILDSTAR 4/5 processing board
- New I/O form factor for improved thermal performance
- First of many WILDSTAR 4/5 Family I/O cards, including superior performance A/D, D/A, and additional high-speed communication cards
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance; WILD solutions outperform the competition

For more information, contact: jdonald@annapmicro.com

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Universal 3Gbit I/O

Annapolis Micro Systems, Inc. is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. The Annapolis Universal 3Gbit IO Card provides up to 36 Gb full-duplex I/O directly between the outside world and the Rocket I/O pins on the Xilinx Virtex-II Pro FPGA processors on the WILDSTAR II Pro main board. No other vendor provides that volume of data straight into the heart of the processing elements and then back out again. The card has three individually configurable, industry standard 4X connectors, providing four lanes per connector, with dedicated signal conditioners to ensure clean communication. It supports a wide variety of readily available cables: copper for short haul (.3-5 m) or fiber for long haul (10-300 m). Two I/O cards can reside on each WILDSTAR II Pro or WILDSTAR II FPGA-based VME or PCI board with up to 30 million user reprogrammable gates.

Initial release of the Universal 3Gbit Card will come with an easy-to-use Rocket I/O protocol supporting up to 12 Gb full duplex per connector. Third quarter 2006 will see releases of up to 10 G full-duplex InfiniBand per connector, up to 10 G full-duplex Ethernet per connector, and Serial FPDP. Although the InfiniBand, Ethernet, and Serial FPDP protocols will be provided as black-box solutions with few modifications by users allowed, more adventurous users who choose to develop their own communications protocols from the basics already have access to all the board resources through a VHDL source for the interfaces to SRAM, Signal Conditioners, LAD Bus, I/O Bus, and PPC Flash. CoreFire users will have the usual CoreFire board support package.

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FEATURES:

- Up to 12 Gb full-duplex Rocket I/O per connector
- Up to 10 Gb full-duplex InfiniBand per connector
- Up to 10 Gb full-duplex Ethernet per connector
- Three individually configurable 4X connectors – four lanes per connector
- Three fundamental oscillators – 100.00 MHz, 125.00 MHz, and 156.25 MHz
- One Xilinx Virtex-II Pro 70-5, -6 or -7, or Industrial 70-5I or 70-6I
- Up to 4 GB DDR2 SDRAM in four banks or up to 1 GB DDR SDRAM in four banks
- Two PowerPC 405s in FPGA with onboard Flash for program storage
- JTAG, ChipScope, and Serial port access
- Proactive thermal management system
- Available in both commercial and industrial temperature grades
- Includes one-year hardware warranty, software updates, and customer support

For more information, contact: jdonald@annapmicro.com

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DR PMC/XMC Digital Receiver

The DR PMC/XMC Digital Receiver PMC card features 16 receiver channels on one card using the most advanced architecture for ultrafast signal capture and real-time processing. It integrates the latest analog chips with a 4M Virtex-II Pro FPGA for user code, ample memory, and flexible clocks/triggers on a 64/66 PCI mezzanine format.

High-speed digital signal processing algorithms in the FPGA are developed using MATLAB and VHDL code. The FPGA framework logic allows quick integration of custom signal processing into the dataflow of the module through use of component-based modular design. DSP algorithms are rapidly designed using high-level MATLAB simulations that can be integrated into the FPGA hardware with minimal VHDL coding.

FEATURES:

- 16 Channel Digital Receiver, 4 A/D 125 MHz
- Virtex-II Pro FPGA, 4 million gates
- PCI 64/66 with P4 port to host card
- 16 MB SDRAM plus 2 MB RAM for FPGA
- Low-jitter PLL clock source
- Advanced SW and firmware demo programs

For more information, contact: sales@innovative-dsp.com

RSC# 31719 @ www.dsp-fpga.com/rsc

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www.innovative-dsp.com

PMC/XMC FPGA Cards

Speed, fidelity, flexibility - The VelociaPMC family integrates ultra-fast signal capture, generation, and co-processing on an advanced PMC architecture. Each card combines new generation analog devices with large user-reconfigurable Virtex-II Pro FPGA, ample DDR memory, low fitter clocks/triggers on a 64/66 PCI with a private JN4 64-bit user I/O port, and a XMC 4-lane Rocket I/O (per VITA 42) that connects straight to the FPGA of our Velocia cPCI boards or other carriers. This ultimate connectivity allows for rapid deployment of the most advanced systems in SDR, signal intelligence, RADAR, and radio test equipment.

The family or cards includes SIO Module Dual 1 Gbps Tx/Rx Serial I/O Ports, DR Module 16 Channel Digital Receiver Card, UWB Ultrwide Digital Receiver, and TX Digital Transmitter.

FEATURES:

- SIO C6416 DSP, 1 GHz – two PowerPC 600 MHz – Xilinx Virtex II Pro – PCI (64/66) XMC (four lanes @ 2.5 Gbps per lane)
- TX four D/A, 16-bit, 1 GHz – two PowerPC, 600 MHz – Virtex II Pro – PCI (64/66) – XMC (four lanes @ 2.5 Gbps per lane)
- UWB two A/D, 12-bit, 250 MHz – two PowerPC, 600 MHz – Virtex II Pro – PCI (64/66) – XMC (four lanes @ 2.5 Gbps per lane)
- DR (Digital Receiver) four A/D, 14-bit, 125 MHz – two PowerPC, 600 MHz – Virtex II Pro – PCI (64/66) – XMC four lane
- Full FPGA dev system (VHDL, MatLab/Simulink) supported by MatLab/Simulink
- Advanced SW and firmware demo programs, with external trigger control

For more information, contact: nhenderson@innovative-dsp.com

RSC# 31717 @ www.dsp-fpga.com/rsc

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TX VelociaPMC

The TX VelociaPMC transmitter card features the most advanced architecture for ultrafast signal generation and real-time processing in wideband radio systems and similar wide spectrum applications. It integrates the latest analog circuit chips with a large FPGA for user code, ample memory, and flexible clocks/triggers on a 64/66 PCI mezzanine format. Novel features include a combination of large, user-programmable FPGA, 1 GSPS DACs, onboard low-jitter PLL clock, Sync Burst RAM dedicated to FPGA for fast, block-oriented processing, and a direct PMC/XMC J4 DIO connection to the host card. This 64-bit J4 interface offers a 1.6 GBps transfer-capable, low-latency connection to Innovative Integration's Velocia series of DSP and FPGA CompactPCI boards.

FEATURES:

- Four AD9779, 16-bit, 1 GSPS converters
- Virtex-II Pro FPGA, 4 million gates
- PCI 64/66 with P4 port to host card
- Low-jitter PLL clock source
- Advanced SW and firmware demo programs

For more information, contact: sales@innovative-dsp.com **RSC# 31718 @ www.dsp-fpga.com/rsc**

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ICS-8554D and 8552B

The ICS-8554D four-channel rugged IF receiver and the ICS-8552B two-channel rugged IF receiver are designed for Software Defined Radio applications in demanding environments. The products include two Graychip GC4016 DDC devices and a 3M gate Xilinx Virtex-II FPGA. The majority of FPGA resources are free for user-defined digital signal processing algorithms.

The ICS-8552B brings high performance to standalone, man-pack applications by including a high-stability (1 PPM) onboard TCXO in addition to two ADC/DDC FPGA channels. The ICS-8554D trades the TCXO for two additional ADCs and is intended for higher channel count in vehicle-mounted systems where a high-precision clock source is externally supplied.

FEATURES:

- Four ADC channels, 14-bits @ 105 MHz, and two ADC channels, 14-bits @ 105 MHz (ADS5424)
- Two Graychip 4016 DDC ASICS and 3M gate Xilinx Virtex-II FPGA
- Simultaneous wideband and narrowband acquisition supported
- ICS-8552B – 1 PPM Temperature Compensated Crystal Oscillator (TCXO) onboard
- 2 MB of FIFO storage
- Pn4 user I/O supports LVTTL or LVDS signaling levels
- Windows, Linux, and VxWorks device drivers

For more information, contact: sales@ics-ltd.com **RSC# 31740 @ www.dsp-fpga.com/rsc**

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WILDSTAR II Pro PCI

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our ninth-generation WILDSTAR II Pro for PCI uses Xilinx's newest Virtex-II Pro FPGAs for state-of-the-art performance. It accepts one I/O card in one, or up to two I/O cards in two, PCI or PCI-X slots, including Dual 1.5 GHz A/D, Dual 1.5 GSps D/A, Quad 105 MHz, Universal 3 Gb (Rocket I/O, 10 GbE, InfiniBand), Quad FC2, Quad GbE, and LVDS. Our boards work on a number of operating systems, including Win NT, 2000, XT, Linux, Solaris, IRIX, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR II Pro for PCI, with its associated I/O Cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

FEATURES:

- One or two Virtex-II Pro Xilinx FPGA processing elements – XC2VP70 or XC2VP100
- Up to 96 MB DDRII or QDRII SRAM
- Up to 512 MB DDR DRAM
- Programmable flash for each processing element to share FPGA images
- Works with PCI or PCI-X backplane
- High-speed DMA multichannel PCI controller
- Host software: Win NT, 2000, XP, Linux, Solaris, DEC Alpha, IRIX, and ALTIX
- Full CoreFire board support package for fast, easy application development
- VHDL model, including source code for hardware interface and ChipScope Access
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: jdonald@annapmicro.com

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WILDSTAR II Pro VME

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our ninth-generation WILDSTAR II Pro for VME uses Xilinx's newest Virtex-II Pro FPGAs for state-of-the-art performance. It accepts up to two I/O cards in one VME slot, including Dual 1.5 GHz A/D, Dual 1.5 GSps D/A, Quad 105 MHz, Universal 3 Gb (Rocket I/O, 10 GbE, InfiniBand), Quad FC2, Quad GbE, and LVDS. Our boards work on a number of operating systems, including Win NT, 2000, XT, Linux, Solaris, IRIX, ALTIX, and VxWorks.

We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on data flow, automatically generates distributed control fabric between cores. Our extensive IP and board support libraries contain more than 1000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven reusable, high-performance IP modules.

WILDSTAR II Pro for VME, with its associated I/O Cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

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FEATURES:

- One to three Virtex-II Pro Xilinx FPGA processing elements – XC2VP70 or XC2VP100
- Up to 144 MB DDRII or QDRII SRAM
- Up to 768 MB DDR SDRAM
- Programmable flash for each processing element to store FPGA images
- Works with VME64x backplane
- High-speed multichannel DMA controller
- Host software: Win NT, 2000, XP, Linux, VxWorks
- Full CoreFire board support package for fast, easy application development
- VHDL model, including source code for hardware interfaces and ChipScope access
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: jdonald@annapmicro.com

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Quadia

Quadia is a quad-DSP, dual FPGA, dual PMC site, CompactPCI board with an advanced architecture that provides the best interprocessor connectivity and access to the finest external interfaces available today, delivering blazing performance and extreme flexibility for advanced signal capture and real-time processing applications.

The board features four C6416 DSPs split in two independent clusters each hosting a PMC site and one large FPGA for end-user code, a central FPGA routing interprocessor communication, end-user FPGA communication, external port serial I/O for PCI Express or other private link, global memory, and PCI interface.

FEATURES:

- 1 GHz TMS320C6416 DSP (x4)
- 64 MB SDRAM per processor
- Flexible internal/external communication mesh
- 64-bit/66 MHz CompactPCI
- Two PMC sites with Jn4 to FPGA
- External data port, up to 12 Gbps

For more information, contact: sales@innovative-dsp.com

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VMETRO Inc.

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Phoenix VPF1

The Phoenix VPF1 is a 6U VME64x data and signal processor supporting VITA 41 backplane switch fabric communications via VXS over P0. The VPF1 comprises four processor nodes: two 1 GHz PowerPC 7447A CPUs and two Xilinx XC2VP70 Virtex-II Pros. Each processor has fully distributed memory, and each FPGA supports multiple inter-node communication channels via RocketIO. These channels bind together local processors and those on separate boards for seamless and scalable processing.

A PMC site, GbE, and P2 resources enable I/O. A comprehensive suite of PowerPC and FPGA tools facilitate rapid development and deployment. Phoenix VPF1s are available in air-cooled or conduction-cooled builds, enabling easy migration from development to production.

FEATURES:

- 2x PowerPC 7447 CPU nodes and 2x Xilinx Virtex-II Pro FPGA nodes
- 8x 2.0-3.125 Gbps off-board serial communications channels
- Ethernet, RS-232, RS-422
- 64-bit, 66 MHz PMC site for local I/O
- VXS (VITA 41) compatible
- Air-cooled and rugged, conduction-cooled build variants

For more information, contact: info@vmetro.com

RSC# 31759 @ www.dsp-fpga.com/rsc

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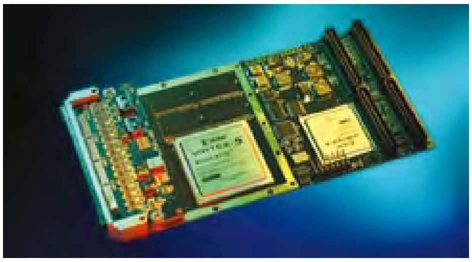
ADM-XRC-5



The ADM-XRC-5 series of FPGA-based PCI Mezzanine Cards exploits the rich feature set of the latest Xilinx Virtex-5 devices. A comprehensive software development kit supports high-performance memory, I/O, and host interfaces.

The ADM-XRC-5 is the ideal COTS solution for prototyping, development, and production deployment.

Applications include radar and sonar processing, Software Defined Radio, reconfigurable computing, telecommunication, encryption/compression, image processing, and Electronic Intelligence (ELINT).

FEATURES:

- Target FPGA: Xilinx Virtex-5 LX110
- Host interface: PMC-X 133 MHz with adapters for PCI-X, CompactPCI, and VXS
- Memory: 1 GB DDR-II SDRAM in four banks
- I/O: XRM adapters for memory, LVDS, CameraLink, FPDP, and analog I/O
- Software: Windows, Linux, and VxWorks API
- Tools: Reference designs and support for Xilinx System Generator

For more information, contact: info@alpha-data.com **RSC# 31701 @ www.dsp-fpga.com/rsc**

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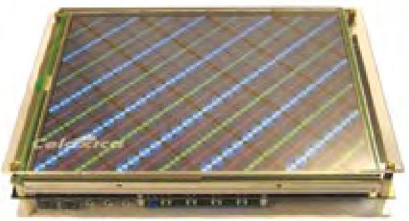
www.celoxica.com

Acceleration Cards



Celoxica algorithm acceleration platforms are based on the latest FPGA devices from Altera and Xilinx and provide all the features needed to prototype complex DSP-based systems.

These high-performance cards, designed for high-speed video and data applications, are optimized for throughput and integration of soft-core microprocessors. The cards come in both desktop and PCI configurations.

In addition, Celoxica provides board support libraries for their powerful C-based synthesis tools to offer a complete algorithm-to-prototype environment from C to FPGA. Software programmers can access all board features using a C-based API.

FEATURES:

- High-performance FPGA devices and peripherals for acceleration of high-speed signal processing applications
- Designed to smoothly off-load processors with FPGA hardware accelerators
- Software programmable using Celoxica C-based synthesis tools
- Supported by extensive software API and IP libraries

For more information, contact: sales@celoxica.com **RSC# 31710 @ www.dsp-fpga.com/rsc**

Annapolis Micro Systems, Inc.
190 Admiral Cochrane Drive, Suite 130 • Annapolis, MD 21401
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www.annapmicro.com

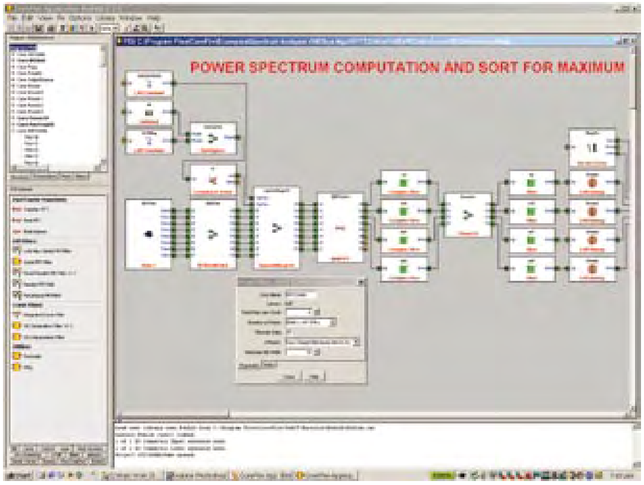
CoreFire FPGA Tool

Develop your application very quickly and easily with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily and quickly build and test their algorithms on the real hardware that will be used in the field.

Use CoreFire's graphical interface to drag and drop library elements onto the design window. Modify your input and output types, numbers of bits, and other core variables by changing module parameters with pull-down menus. The modules automatically provide correct timing and clock control. Insert debug modules to report actual hardware values for hardware-in-the-loop debugging. Hit the Build button to check for errors and as-built core sizes and to build an encrypted EDIF file. Use the Xilinx ISE tool to place and route each FPGA design. Modify and use the jar file or the C program created by the CoreFire Build to load your new file into your WILDSTAR II and I/O card hardware. Use the CoreFire Debugger to view and modify register and memory contents in the FPGA and to step through the dataflow of your design running in the real physical hardware.

Our extensive IP and board support libraries contain more than 1,000 proven, reusable high-performance cores, including FIR and CIC filters, a channelizer, and the world's fastest FFT. We support conversion between data types: bit, signed and unsigned integers, single precision floating point, integer and floating point complex, and arrays. A few of the newly added array cores include array composition and decomposition; slice, parallelize, serialize, repack, split, merge, reorder, rotate, and concatenate transformations; matrix math, sliding windows, and convolutions.

The combination of our COTS hardware and CoreFire enables our customers to make massive improvements in processing speed while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.



FEATURES:

- Dataflow-based – automatically generates inter-module control fabric
- Drag and drop graphical interface
- Work at high conceptual level – concentrate on solving algorithmic problems
- Hardware-in-the-loop debugging
- More than 1,000 modules incorporate years of application experience
- Reduce risk with COTS boards and software
- Save time to market
- Save development dollars
- Easily port completed applications to new technology chips and boards
- Training and custom application development available
- Achieve world-class performance – WILD solutions outperform the competition
- Annual node locked or networked license; includes customer support and updates

For more information, contact: jdonald@annapmicro.com

RSC# 19250 @ www.dsp-fpga.com/rsc

Celoxica

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CtoFPGA Synthesis

Celoxica provides complete design environments for synthesis of C algorithms to FPGA hardware from both Handel-C and SystemC. Celoxica is the leading supplier of C-based design and synthesis tools, specializing in digital imaging and signal processing applications.

Celoxica C-synthesis produces optimal design partitions and quality results, maximizes design productivity, and directly implements complex DSP software to FPGA and RTL.

Celoxica's proven technology has been used in thousands of designs to accelerate system performance, cutting design cycles in half and turning software algorithms into FPGA silicon.

FEATURES:

- Direct synthesis from Handel-C (synthesizable ANSI-C) or SystemC models to FPGA gates
- Fast cycle-accurate simulation of system models in C, C++, Handel-C, or SystemC; co-simulation with RTL and MATLAB models
- Rapid partioning of algorithms between processors and FPGA hardware; integration with popular processors
- Generation of human readable RTL models and integration with common ASIC tool flows

For more information, contact: sales@celoxica.com RSC# 31709 @ www.dsp-fpga.com/rsc

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Lyrtech

4495 Wilfrid Hamel Blvd. Suite 100 • Quebec, PQ G1P 2J7 Canada
Tel: 888-922-4644 • Fax: 418-877-7710
www.lyrtech.com/vhs-adc-v4/virtex.php

VHS-ADC Virtex-4

Lyrtech introduces the VHS-ADC Virtex-4, a high-speed, multichannel acquisition card. It is equipped with eight phased-synchronous ADC that operate at a maximum rate of 105 MHz and a high-capacity Virtex-4 FPGA for high-speed processing. It also comes with SDRAM for data storage, an expansion mezzanine connector to add eight additional input channels, eight additional output channels, or additional SDRAM memory for recording and playback. It supports the combination of System Generator form DSP fom Xilinx and Simulink tools for model-based design. This makes the VHS-ADC Virtex-4 perfect for multichannel intermediate frequency processing, smart or array antennas, multiple in/multiple out (MIMO) development, and more.

FEATURES:

- High-speed multichannel acquisition board featuring eight synchronous, 14-bit, 105-MSPS ADC
- Outstanding clock synchronization: very-low-skew inter-channel clock routing through all the ADC
- Virtex-4 FPGA, processing up to 512 XtremeDSP slices with Xilinx Virtex-4 (SX55, LX100, or LX160 support)
- Flexible graphical user interface, API and drivers, and expansion mezzanine connector for 8 more ADC or DAC
- Model-based design support (Xilinx System Generator for DSP)
- 128-MB FPGA external SDRAM with recording/playback software tools

For more information, contact: marie-sophie.roussin@lyrtech.com RSC# 31727 @ www.dsp-fpga.com/rsc

Synplicity, Inc.
600 West California Avenue • Sunnyvale, CA 94086
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www.synplicity.com

Synplicity®
Simply Better Results

Synplify DSP

Advanced FPGAs are the perfect vehicle for high performance DSP applications. Hundreds of millions operations per second can be achieved, and dedicated DSP blocks and multipliers facilitate efficient and parallel implementation of DSP functions. However the traditional implementation path of hand-coding the RTL often is error-prone and time consuming, with numerous iterations between the algorithm architect and the hardware designer. With Synplify DSP you can model and simulate your algorithms quickly, and automatically create optimized RTL implementations for a wide range of target devices.

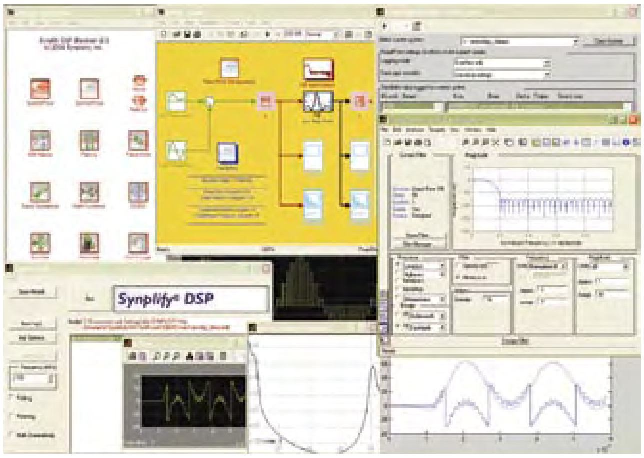
Automated RTL implementation – The Synplify DSP product automatically generates RTL and a verification test bench from a Simulink system-level specification. No hand-coding of any RTL is required.

The Synplify DSP blockset – Synplify DSP provides a set of functional blocks commonly used in DSP design including filtering (FIR, IIR), transforms, math functions, CORDIC, signal operations, memories, and control logic. These functions are technology-independent and tightly integrated into The MathWorks environment, allowing the algorithm designer to utilize Simulink features such as discrete-time simulation, multi-rate management, fixed point quantization, scope debugging, and more.

FPGA hardware independence – Synplify DSP allows algorithm behavior to be captured in Simulink without preselecting the specific FPGA device for implementation. The Synplify DSP toolbox automatically implements an optimized architecture in RTL based upon your timing and area requirements.

Multi-channel system from single-channel specification – Synplify DSP enables quick what-if analysis on channel capacity by automatically generating a pipelined system from a single channel specification.

Area-speed tradeoffs – Math intensive DSP algorithms easily consume large numbers of expensive hardware functions such as multipliers. The Synplify DSP tool analyzes the design to automatically find opportunities for sharing these resources, saving design iterations and significant area.



FEATURES:

- Rapidly create high-level, technology independent DSP models with fully integrated Synplicity fixed-point DSP library
- High quality RTL code and testbench automatically synthesized from Simulink model
- DSP synthesis – DSP architecture optimizations such as system-level re-timing for performance and folding for area utilization
- Extensive floating-point to fixed-point conversion and analysis
- Vector support – concise expression of parallel and multi-channel operations
- Powerful system-wide optimizations for performance, area, and multi-channelization tradeoffs
- Technology independence allows targeting any FPGA architecture from the same Simulink model
- M-control – use a subset of M-language to describe complex state machine and control logic
- Multi-channelization – automatically produces a resource optimized multi-channel implementation from a single channel specification
- Integrated quantization and multi-rate analysis – accelerate design and verification of fixed-point multi-rate DSP algorithms
- Automatic datatype propagation propagates type and adjusts word width to avoid overflow saving manual calculation and implementation
- Synplify DSP blockset – hardware abstraction focuses on algorithm behavior, separates implementation details and enables full portability

For more information, contact: info@synplicity.com

RSC# 31750 @ www.dsp-fpga.com/rsc

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Synplicity
Simply Better Results

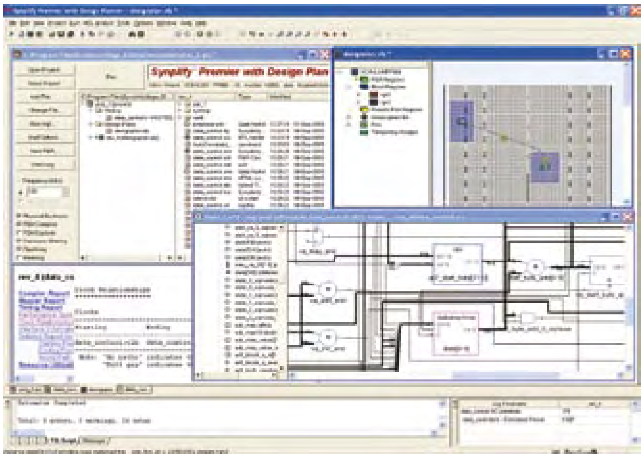
Synplify Premier

Synplicity's Synplify Premier software is the ultimate FPGA synthesis and debug solution. It builds upon Synplicity's industry-leading synthesis technology, and adds new graph-based physical synthesis for timing closure and simulator-like visibility into operating FPGA devices for fast source-level debug.

Graph-based physical synthesis – Synplicity invented graph-based physical synthesis to improve timing closure by means of a single-pass physical synthesis flow for 90 nm FPGAs. In FPGAs, unlike ASICs, proximity of placed logic does not imply better timing. The essence of the graph-based approach is that pre-existing wires, switches, and placement sites used for routing an FPGA can be represented as a detailed routing resource graph. The notion of distance then changes to a measure of delay and availability of wires. The Synplify Premier tool's graph-based physical synthesis technology merges optimization, placement, and routing to generate a fully placed and physically optimized netlist, providing rapid timing closure and a 5 percent to 20 percent timing improvement.

Best quality of results – The Synplify Premier product is a true timing-driven synthesis product, which means it delivers the timing performance you need in your design by automatically moving registers within combinatorial logic in order to balance timing delay and improve circuit performance up to an additional 20 percent Quality of Results (QoR).

Simulator-like visibility into a live FPGA – The Synplify Premier software provides a rapid method of finding functional errors in FPGA designs by providing simulator-like visibility into operating FPGA hardware. Synplicity's integrated debugging software, based upon technology from the Identify product, allows designers to annotate signals and conditions they want to monitor directly in their RTL code.



FEATURES:

- Graph-based physical synthesis – fast timing closure and a push-button performance boost of up to 20 percent
- True timing-driven synthesis – after meeting timing constraints, automatically optimizes your design for area/cost
- Automatic handling of DSP functions – infers DSP functions from RTL and maps into vendor's DSP hardware (i.e. MACs)
- Lightning-fast compile times – synthesizes even the largest design in a fraction of the time of other tools
- HDL analyst RTL analysis and debugging tool – instantly generates RTL block diagrams from your RTL code; helps identify critical paths
- Interactive timing analysis – enables point-to-point timing analysis without re-synthesis
- Automatic RAM inferencing – bypass tedious hand instantiation of RAM and makes your design technology independent
- FSM explorer – automatically finds and selects the best FSM coding style for the meeting your timing and area constraints
- Automatic retiming – moves registers automatically within combinatorial logic to balance delay and improve performance
- Integrated RTL instrumentation and debug – instrument and debug your design directly in your RTL source code
- Probe point creation v allows any signal to be tied to an external pin for testing without HDL code changes

For more information, contact: info@synplicity.com **RSC# 31749 @ www.dsp-fpga.com/rsc**

Integrated Device Technology, Inc. (IDT)

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www.IDT.com

IDT70K2000 PPS

As wireless infrastructures evolve toward higher performance 3G systems and beyond, designers must process more carriers and sectors per base station to deliver significant cost reductions to the consumer. As such, their designs must be flexible and scalable to quickly meet the growing needs of this market segment. Functions such as within-packet manipulation and summing, and muxing of channels can consume large amounts of system resources and add latency to the system. While many have turned to custom solutions, including FPGA and ASIC implementations, IDT has reduced or eliminated the risks and higher costs associated with these alternatives, with an innovative standards-based solution.

A first in the industry, the IDT IDT70K2000 serial RapidIO pre-processing switch (PPS) targeting digital signal processor (DSP) clusters accelerates wireless baseband processing applications, while supporting the serial RapidIO interconnect specifications. The product integrates a suite of byte- and packet-level manipulation capabilities designed to offload bandwidth intensive tasks from the DSPs, allowing wireless base station designers to create scalable, flexible, and cost-effective solutions. The result can be an acceleration of each DSP in a cluster by up to 20 percent, enabling the DSPs to focus on other compute-intensive functions in wireless base stations.

The IDT70K2000 is central to the DSP Farms' processing architecture. It performs a variety of data processing on the payload of sample packets to accelerate the subsequent algorithmic operations of a receiving processor (DSP, CRP, FPGA). It also supports serial RapidIO packet switching (unicast, multicast, or broadcast) from any input to any output port. Enabling acceleration of baseband processing in support of a variety of wireless standards, it may also be used for radio network controllers and media gateway applications, video imaging in medical equipment, high-end surveillance, or similar signal processing-intensive applications.

FEATURES:

- Optimized as board-level switching solution, supporting tailored distribution of data to multiple DSPs
- Enables reduction of DSP/CRP cycles by 20 percent or more by offloading low value or duplicated tasks, while enabling maximized efficiency
- Enables addition of more channels, more users at a fixed cost
- Features scalable serial RapidIO links to address a wide range of wireless and non-wireless applications
- Provides distribution of processed data via unicast, multicast, or broadcast operations
- Includes 40 bidirectional serial RapidIO lanes, configurable to support up to 22 1x ports, or 10 4x ports (or multiple combinations)
- Allows each port's speed, width, and reach to be independently configured
- Supports within sample processing operations, including endian conversions, and alignment of sample length
- Supports within-packet processing, including re-sequencing samples, placing them into separate specific locations in the memory (DMA)
- Provides summation across input ports of up to 22 packets and allows TDM-like synchronization of packets from multiple ports
- Package: 676-ball grid array, 27 mm x 27 mm, 1.0 mm ball pitch
- Available on AMC form-factor evaluation boards connecting four TI-6455 or -6482 DSP

For more information, contact: flow-controlhelp@idt.com

RSC# 31724 @ www.dsp-fpga.com/rsc

Annapolis Micro Systems, Inc.
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Dual 1.5 GHz A/D

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. The Annapolis Dual 1.5 GHz A/D I/O card provides two channels of 1.5 GSps input (with 8-bit resolution) or one channel of 3.0 GSps input (with 8-bit resolution). The board has two Max108 8-bit ADCs, each one fed by its own pair of differential signals. The differential clock signals coming into the board can provide identical clocks to both A/Ds for dual 1.5 GSps channels or an inverted clock to one of the A/Ds to interleave the data for a single 3.0 GSps channel. Multiple I/O cards can be synched together via the Annapolis Clock Sync Distribution Board, as in the 24 GSps A/D Collection, Processing, and Distribution (CPD) systems.

The Xilinx Virtex-II Pro 70 on the board provides user-configurable, real-time continuous sustained processing of the full data stream. Up to two of these I/O cards can reside on the Annapolis WILDSTAR II or WILDSTAR II Pro FPGA-based VME and PCI bus boards, which provide up to 30 million more user-reprogrammable FPGA gates for onboard processing.

Our boards run on many different operating systems. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models. VHDL source is provided for interfaces to SRAM, LAD bus, I/O bus, and DACs. CoreFire users will have the usual CoreFire board support package. Annapolis is famous for the high quality of our products and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training and exceptional special application development support, as well as more conventional support.

FEATURES:

- Two MAX 108 8-bit A/D converters – two 1.5 GSps channels or one 3 GSps channel
- Two sets of differential or single-ended input signals – one for each A/D
- Differential or single-ended clock input – synchronize or interleave the two data streams
- Up to 4 GBps I/O bandwidth to WILDSTAR II Pro motherboard I/O slot
- Xilinx Virtex-II Pro XC2V70 FPGA for user-reprogrammable processing
- Heat sink on A/Ds; heat sink/fan in PCI chassis
- Host software: Win NT, 2000, XP, Linux, VxWorks, Solaris, DECAlpha, and SGI
- Full CoreFire board support package for fast, easy application development
- VHDL model, including source code for board level interfaces and ChipScope access
- Save time and effort and reduce risk with COTS boards and software
- Achieve world-class performance – WILD solutions outperform the competition
- Includes one-year hardware warranty, software updates, and customer support; training available

For more information, contact: jdonald@annapmicro.com

RSC# 19249 @ www.dsp-fpga.com/rsc

Traquair Data Systems, Inc.
114 Sheldon Rd • Ithaca, NY 14850 USA
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www.traquair.com

ORS-11x Analog/FPGA Boards

ORS-11x analog/FPGA boards combine high-performance, multi-channel analog interfaces with a user-programmable Spartan-IIE or Virtex-II FPGA, providing developers with the means to implement FPGA-based digital signal processing solutions. They can be used as stand-alone devices with the user-programmable FPGA responsible for supporting all signal processing functionality, or as daughtercards to micro-line DSP/FPGA boards.

A variety of multi-channel A/D/A configurations are supported: 2-channel 14-bit A/D/A with ADC sample rates up to 65 MSps; 4-channel 16-bit A/D/A with ADC sample rates up to 2.5 MSps; 12-channel A/D/A with ADC sample rates up to 250 KSps.

If the capabilities of a Texas Instruments TMS320C6000 DSP processor are required, an ORS-11x board can be fitted as a daughtercard to a TMS320C6000-based micro-line embedded DSP/FPGA board. micro-line embedded DSP/FPGA boards combine the latest TMS320C6713 floating point and TMS320C64xx integer DSP processors with user-programmable high density FPGAs, in small, cost-optimized configurations.

VHDL FPGA programming packages are available for all ORS-11x board configurations, allowing users to implement custom logic or processing algorithms. Support for Xilinx System Generator for DSP and Matlab Simulink is also being introduced, and is already available as an option for the ORS-114. System Generator for DSP, the Simulink add-on from Xilinx, takes a graphical approach to algorithmic design and extends Simulink for FPGA development.

ORS-114

FEATURES:

- ORS-112 (16-bit A/D/A)
  - Four simultaneously sampled 16-bit ADC inputs, at up to 2.5 MSps per channel
  - ADC inputs use Analog Devices AD9260 over-sampling converters
  - Four simultaneously sampled 16-bit DAC outputs, with 10 usec settling time to 0.0015% FSR
  - Programmable 200 KGate Spartan-IIE or 500 KGate Virtex-II FPGA
- ORS-114 (14-bit A/D/A)
  - Two simultaneously sampled 14-bit ADC inputs, at up to 65 MSps
  - Two simultaneously sampled 14-bit DAC outputs, with 35 nsec settling time to 0.1% FSR
  - Programmable 1 MGate Virtex-II FPGA
- ORS-116 (16-bit A/D/A)
  - Twelve simultaneously sampled 16-bit ADC inputs, at up to 250 KSps per channel
  - Twelve simultaneously sampled 16-bit DAC outputs, with 10 usec settling time to 0.003% FSR
  - Programmable 200KGate Spartan-IIE FPGA

For more information, contact: mhl@traquair.com

RSC# 31753 @ www.dsp-fpga.com/rsc

VMETRO

1880 S. Dairy Ashford, Suite 400 • Houston, TX 77077
Tel: 281-584-0728 • Fax: 281-584-9034
www.vmetro.com

PMC-FPGA05 Module

The PMC-FPGA05 is a Xilinx Virtex-5 XC5VLX110 platform FPGA-based, PMC module with high-speed digital I/O and PCI-X interface to the host computer. Three banks of 2 Mb x 18 (4 MB) QDR II SRAM support DSP functions in the Virtex-5. Two independent banks of 512 Mb x 16 (64 MB) DDR2 SDRAM are directly connected to the FPGA. There are 138 signals routed to a 180-way connector near the front panel. These lines are routed so that they may be used as single-ended signals or differential pairs. I/O modules available include ADC, DAC, LVDS, FPDP II, CameraLink, and RS-422.

Example VHDL code blocks are provided to show how the PMC-FPGA05 resources can be used, along with utilities for configuring flash. The PMC-FPGA05 is supported under Windows XP.

FEATURES:

- Xilinx Virtex-5 LX110 FPGA
- Multiple banks of SRAM for DSP
- Multiple banks of SDRAM for large buffers
- Customizable digital I/O or choose an I/O module for ADC, DAC, LVDS, FPDP II, CameraLink, or RS-422
- PCI-X interface
- Windows XP support

For more information, contact: info@vmetro.com

RSC# 31758 @ www.dsp-fpga.com/rsc

Radstone Sensor Processing

296-300 Concord Road, Corporate Center, Suite 120
Billerica, MA 01821
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www.radstone.com

ICS-645B

Derived from the popular ICS-645 product, the ICS-645B offers a cost effective solution for high frequency (littoral and mine hunting) and test and measurement (vibration analysis and jet engine testing) applications.

The ICS-645B provides synchronous sampling at up to 20 MSps across all channels. It also features 16 MB of onboard storage, making it ideal for transient capture and high data throughput applications using non real-time operating systems such as Windows or Linux. The ICS-645B is a direct replacement for the earlier ICS-645 product providing a 4x improvement in PCI throughput and memory capacity, and 2.5x improvement in FPDP throughput.

FEATURES:

- Full length (long) PCI form factor
- 32 16-bit ADC channels sampling at up to 20 MSps
- 8x, 4x, 2x, 1x oversampling modes
- 64-bit, 66 MHz PCI interface (PCI 2.2 compliant), universal signaling – 400 MBps FPDP II interface
- Simultaneous sampling across all channels, even in multi-card systems and 16 MB of onboard storage
- Windows, Linux device drivers and MatLab libraries available

For more information, contact: sales@ics-ltd.com

RSC# 31739 @ www.dsp-fpga.com/rsc

Traquair Data Systems, Inc.
114 Sheldon Rd • Ithaca, NY 14850
Tel: 607-266-6000 • Fax: 607-266-8221
www.traquair.com

ultra-compact DSP/FPGA MCMs

The ultra-compact UC1394a-1 and UC1394a-3 multi-chip modules provide Texas Instruments TMS320C5000 DSP, Spartan-II or Spartan-3 FPGA, and ready-to-use IEEE1394a FireWire communication capabilities in tiny 30 mm x 36 mm surface-mount PLCC packages. They are suitable as user-programmable DSP/FPGA resources or as FireWire connectivity devices.

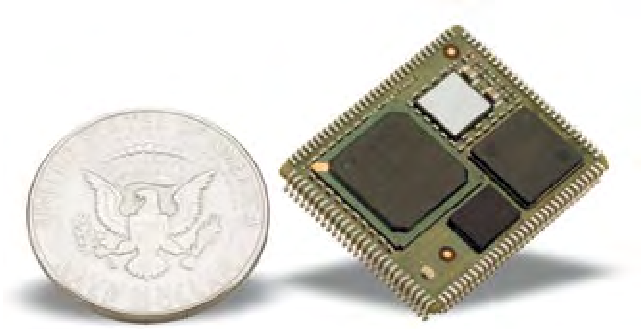
The UC1394a-1 incorporates a TMS320C5509 integer DSP, a 50 KGate Spartan-II FPGA, 8 MB of SDRAM. In addition to the I/O capabilities of the UC1394a-3, the UC1394a-1 provides external access to USB and four A/D inputs provided by the TMS320C5509 DSP processor.

The UC1394a-3 incorporates a TMS320C5501 integer DSP and a 50 KGate Spartan-3 FPGA (or TMS320C5502 integer DSP and a 200 KGate Spartan-3 FPGA), as well as 4 MB of SDRAM and a wide variety of additional I/O capabilities that include RS-232, I2C, McBSP, JTAG, and user-configurable digital I/O via the FGPA. Both the UC1394a-1 and the UC1394a-3 have dedicated FireWire interfaces and 512 KB of boot program FLASH ROM.

User-Programmable DSP and FPGA – the DSP and FPGA are both user programmable, allowing the modules to be used as tiny embedded DSP boards, with the FireWire and other I/O interface options being used as needed.

Ready-to-Use FireWire – a ready-to-use FireWire interface can be used with very little effort as a means for integrating digital cameras, sensors, and other embedded devices within a high-performance FireWire network. DSP and FPGA programming is not required for simple FireWire bridging functionality, greatly reducing development time.

EVM Development Kits – EVM development kits are available for: (a) DSP programming, with options for FGPA programming, FireWire video frame capture, and enabling digital cameras for FireWire IIDC DCAM v1.3 compatibility; and (b) for enabling sensors and other embedded devices for FireWire operation without the need for DSP or FPGA programming.



FEATURES:

- UC1394a-1
  - TMS320C5509 integer DSP
  - 50 KGate Spartan-II FPGA
  - 21 FPGA I/O pins for streaming interface; 27 additional I/O pins for user-configurable I/O
  - 2-port 400 Mbps IEEE1394a FireWire interface
  - 8 MB SDRAM; 512 KByte boot program FLASH ROM
- UC1394a-3
  - TMS320C5501 integer DSP with 50 KGate Spartan-3 or TMS320C5502 integer DSP with 200 KGate Spartan-3
  - 21 FPGA I/O pins for streaming interface or as user-configurable I/O
  - 2-port 400 Mbps IEEE1394a FireWire interface
  - 4 MB SDRAM; 512 KByte boot program FLASH ROM

For more information, contact: mhl@traquair.com

RSC# 31752 @ www.dsp-fpga.com/rsc

Annapolis Micro Systems, Inc.
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www.annapmicro.com

WILDSTAR 4 for PCI

Annapolis Micro Systems is a world leader in high-performance, COTS FPGA-based processing for radar, sonar, SIGINT, ELINT, DSP, FFTs, communications, Software-Defined Radio, encryption, image processing, prototyping, text processing, and other processing intensive applications. Our 10th-generation WILDSTAR 4 for PCI-X uses Xilinx's newest Virtex-4 FPGAs for state-of-the-art performance. It accepts one I/O card in one, or up to two I/O cards in two, PCI-X slots, including single 1.5 GHz 8-bit ADC, quad 250 MHz 12-bit ADC, dual 2.3/1.5 GSps 12-bit DAC, Universal 3 Gbit serial I/O (Rocket I/O, 10 GbE, InfiniBand), and Tri XFP (10 GbE, 10G FC). Our boards work on a number of operating systems, including Windows, Linux, ALTIX, and VxWorks. We support our board products with a standardized set of drivers, APIs, and VHDL simulation models.

Develop your application very quickly with our CoreFire™ FPGA Application Builder, which transforms the FPGA development process, making it possible for theoreticians to easily build and test their algorithms on the real hardware that will be used in the field. CoreFire, based on dataflow, automatically generates distributed control fabric between cores.

Our extensive IP and board support libraries contain more than 1,000 cores, including floating point and the world's fastest FFT. CoreFire uses a graphical user interface for design entry, supports hardware-in-the-loop debugging, and provides proven, reusable, high-performance IP modules. WILDSTAR 4 for PCI-X, with its associated I/O cards, provides extremely high overall throughput and processing performance. The combination of our COTS hardware and CoreFire allows our customers to make massive improvements in processing speed, while achieving significant savings in size, weight, power, person-hours, dollars, and calendar time to deployment.

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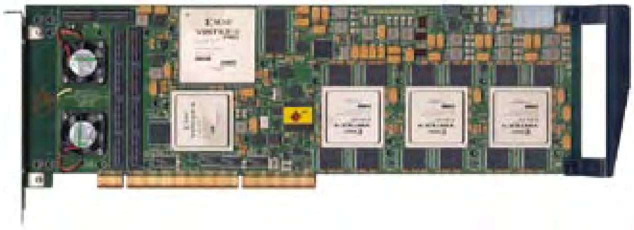

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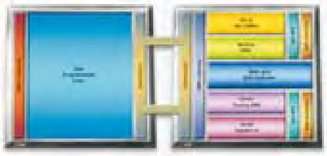

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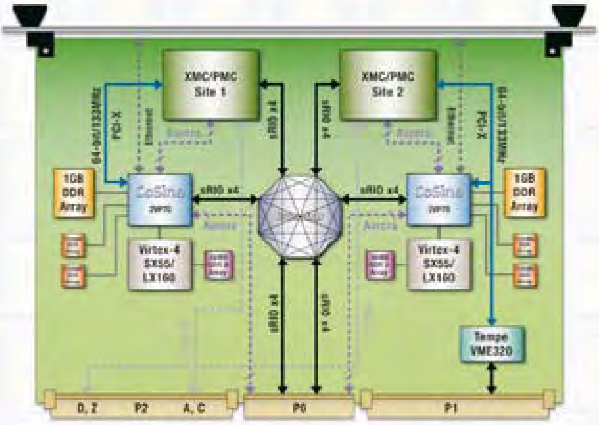

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